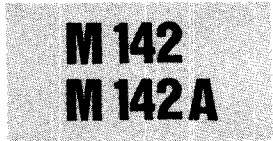


MOS INTEGRATED CIRCUITS



PRELIMINARY DATA

QUAD 80-BIT STATIC SHIFT REGISTER

- SINGLE VOLTAGE SUPPLY: $V_{CC} = 5V \pm 5\%$
- DC to 3 MHz OPERATION GUARANTEED
- FULLY TTL COMPATIBLE
- FULLY DC OPERATION
- SINGLE LINE CLOCK
- PIN-FOR-PIN REPLACEMENT for MK 1007P-TMS 3409 - 2532 - 3347
- LOW POWER DISSIPATION : 250 mW (TYP.)
- INPUT GATE PROTECTION
- M 142A IS A HIGH SPEED SELECTION

The M 142 and M 142A are quad 80-bit fully DC shift register constructed on a single chip using very low threshold N-channel silicon gate technology which allows high speed (3 MHz guaranteed) and fully TTL compatibility without using any external resistor.

Each of the four 80-bit registers has an independent input, output and recirculate control. The single clock line is common to all four registers.

Transferring data into the register is accomplished when the clock is high (logic "1") Shifting of data occurs when the clock goes low. Output data appears on the negative going edge of the clock.

When the recirculate line is high, data recirculates, while input is inhibited. When data is entered, the recirculate line is at logic "0".

Output data attain the same logic state that was shifted into the register 80 clocks prior. Available in 16-lead dual in-line plastic or ceramic package.

ABSOLUTE MAXIMUM RATINGS

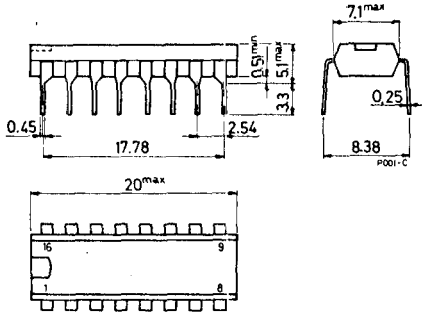
V_{CC}	Supply voltage	-0.5 to 7	V
V_i	Input voltage on any pin	-0.5 to 7	V
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature	0 to 70	°C

ORDERING NUMBERS: M 142 B1 for dual in-line plastic package
M 142 D1 for dual in-line ceramic package
M 142A B1 for dual in-line plastic package
M 142A D1 for dual in-line ceramic package

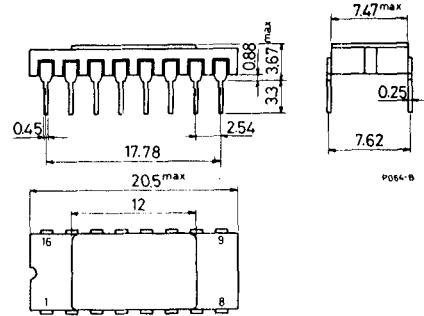
M 142 M 142A

MECHANICAL DATA (dimensions in mm)

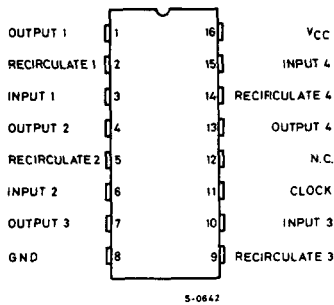
Dual in line plastic package for
M 142 D1 and 142A D1



Dual in line ceramic package for
M 142 B1 and M 142A B1

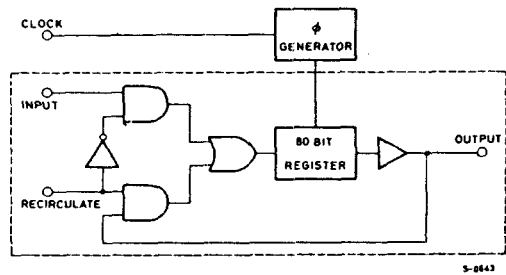


CONNECTION DIAGRAM



BLOCK DIAGRAM

(one of four shown)



M 142 M 142A

TRUTH TABLE (positive logic)

Recirculate	Input	Function
"0"	"0"	"0" is written
"0"	"1"	"1" is written
"1"	"0"	Recirculate
"1"	"1"	Recirculate

"0" = 0V, "1" = 5V

STATIC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $T_{amb} = 0$ to $70^{\circ}C$ unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}^* Input high voltage		2		V_{CC}	V
V_{IL}^* Input low voltage		-0.3		0.8	V
V_{OH} Output high voltage	$I_{OH} = -100 \mu A$	2.4			V
V_{OL} Output low voltage	$I_{OL} = 1.6 \text{ mA}$			0.4	V
I_{LI}^* Input leakage current	$V_i = V_{CC}$			1000	nA
I_{CC} Supply current			48		mA

* These parameters apply to all inputs including clock

DYNAMIC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $T_{amb} = 0$ to $70^{\circ}C$) unless otherwise specified)

Parameter	Test conditions	Min.	Typ.	Max.	Unit
f Clock repetition rate				3	MHz
$t_{\phi_{pw1}}$ Clock high pulse width		110			ns
$t_{\phi_{pw0}}$ Clock low pulse width		220			ns
t_r, t_f Clock rise and fall time				5	μs
t_s Set-up time		100			ns
t_h Hold time		80			ns
t_{sR} Recirculate set-up time		100			ns
t_{hR} Recirculate hold time		80			ns
t_{Dr}, t_{Df} Delay time to rise and fall	TTL load for M 142 type $C_L = 10 \text{ pF}$ for M 142A type			230	ns
C_{iR} Recirculate input capacitance	$V_i = 0V, f = 1 \text{ MHz}$			160	ns
C_{ϕ} Clock capacitance	$V_{\phi} = 0V, f = 1 \text{ MHz}$			8	pF
				12	pF

M 142 M 142A

WAVEFORMS

