

HIGH SPEED 1K X 8 DUAL-PORT STATIC SRAM

Features

- High-speed access
 - Military: 25/35/55/100ns (max.)
 - Industrial: 55/100ns (max.)
 - Commercial: 20/25/35/55/100ns (max.)
- Low-power operation
 - IDT7130/IDT7140SA Active: 550mW (typ.) Standby: 5mW (typ.)
 - IDT7130/IDT7140LA Active: 550mW (typ.) Standby: 1mW (typ.)
- MASTER IDT7130 easily expands data bus width to 16-ormore-bits using SLAVE IDT7140

- On-chip port arbitration logic (IDT7130 Only)
- BUSY output flag on IDT7130; BUSY input on IDT7140
- INT flag for port-to-port communication
- Fully asynchronous operation from either port
- Battery backup operation-2V data retention (LA only)
- TTL-compatible, single 5V ±10% power supply
- Military product compliant to MIL-PRF-38535 QML
- Industrial temperature range (-40°C to +85°C) is available for selected speeds
- Available in 48-pin DIP and LCC, 52-pin PLCC, and 64-pin STQFP and TQFP
- ŌĒR OEL CE CER R/W R/WR 1/00L-1/07L I/OOR-I/O7R I/O I/O Control Control BUSYL^(1,2) $\overline{\text{BUSY}}_{\text{R}}^{(1,2)}$ A9L A9R Address MEMORY Address • ě Decoder ARRAY Decoder AOL AOR ARBITRATION CEL 2 ₹ CER and INTERRUPT OEL ₹ **₹**0ER LOGIĆ R/WL Ł ₹R/WR ► INT⁽²⁾ 2689 drw 01

NOTES:

- 1. IDT7130 (MASTER): BUSY is open drain output and requires pullup resistor.
- IDT7140 (SLAVE): BUSY is input.
- 2. Open drain output: requires pullup resistor.

JUNE 2000

Functional Block Diagram

Military, Industrial and Commercial Temperature Ranges

Description

The IDT7130/IDT7140 are high-speed 1K x 8 Dual-Port Static RAMs. The IDT7130 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7140 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-ormore-bit memory system applications results in full-speed, errorfree operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by \overline{CE} , permits the on chip circuitry of each port to enter a very low standby power mode.

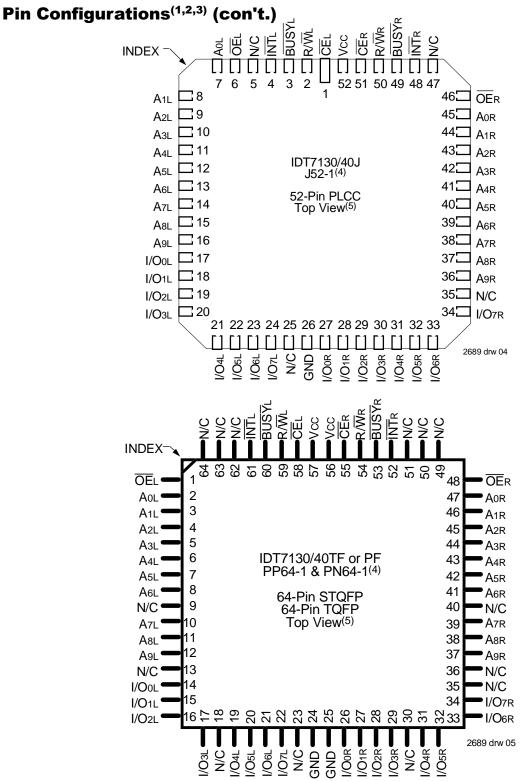
Fabricated using IDT's CMOS high-performance tech-nology, these devices typically operate on only 550mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT7130/IDT7140 devices are packaged in 48-pin sidebraze or plastic DIPs, LCCs, flatpacks, 52-pin PLCC, and 64-pin TQFP and STQFP. Military grade products are manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

CEL 48 1 Vcc <u>R/W</u>∟ 47 CER 2 BUSYL 3 46 R/WR INTL 4 45 BUSYR OEL 5 44 INTR AOL 6 43 OER A1L 7 42 AOR 8 A2L IDT7130/40 P or C P48-1⁽⁴⁾ 41 A1r АзL 9 40 A2R 39 A4L 10 A3R & C48-2⁽⁴⁾ A5L 11 38 A4r A6L A5r 12 37 48-Pin DIP A7L 13 36 A6R 14Top View⁽⁵⁾ 35 A8L A7r 34 A9l 15 A8R 33 I/OOL 16 A9R 32 I/O1L /cc ЫЩ 17 I/O7r INDEX 31 I/O_{2L} 18 I/O6r m I/O3L 19 30 I/O5r 20 29 I/O4L I/O4r 5 4 3 2 48 47 46 45 44 43 6 I/O5L 21 28 I/O3r 1 A1L Aor 22 27 I/O6L I/O2R 38 41 A2L A1r I/O7∟ 23 26 I/O1r GND 24 I/OOR 25 9 40 A2r Азь 2689 drw 02 10 39 A4L Азr IDT7130/40L48 or F]11 L48-1⁽⁴⁾ 38 A5L A4R & 12 37 A6L A5r F48-1⁽⁴⁾ A7L 13 36 A6R 48-Pin LCC/ Flatback 314 35 A7R A8L Top View⁽⁵⁾ 315 34 A9L A8r I/OOL 316 33 A9r NOTES: 317 I/O1L 32 I/O7R 1. All Vcc pins must be connected to power supply. 18 31 I/O2L 2. All GND pins must be connected to ground supply. I/O6R P48-1 package body is approximately .55 in x .61 in x .19 in. 19 20 21 22 23 24 25 26 27 28 29 30 3 C48-2 package body is approximately .62 in x 2.43 in x .15 in. L48-1 package body is approximately .57 in x .57 in x .68 in. /05r 2689 drw 03 GND /Oor /01R /O3R /04r F48-1 package body is approximately .75 in x .75 in x .11 in. /O2R 1/05L 140/1 190/I This package code is used to reference the package diagram. 4 This text does not indicate orientation of the actual part-marking. 5.

Pin Configurations^(1,2,3)

Military, Industrial and Commercial Temperature Ranges



- 1. All Vcc pins must be connected to power supply.
- 2. All GND pins must be connected to ground supply.
- J52-1 package body is approximately .75 in x .75 in x .17 in. PP64-1 package body is approximately 10 mm x 10 mm x 1.4mm. PN64-1 package body is approximately 14mm x 14mm x 1.4mm.
- 4. This package code is used to reference the package diagram.
- 5. This text does not indicate orientation of the actual part-marking.

Absolute Maximum Ratings⁽¹⁾

Symbol	Rating	Commercial & Industrial	Military	Unit
Vterm ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
Tbias	Temperature Under Bias	-55 to +125	-65 to +135	٥C
Tstg	Storage Temperature	-65 to +150	-65 to +150	٥C
Ιουτ	DC Output Current	50	50	mA
NOTEC				2689 tbl 01

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- 2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to \leq 20mA for the period of VTERM \geq Vcc + 10%.

Capacitance (TA = +25°C, f = 1.0MHz) STQFP and TQFP Packages Only

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
Cin	Input Capacitance	ViN = 3dV	9	pF
Соит	Output Capacitance	Vout = 3dV	10	pF
				2689 tbl 05

NOTES:

1. This parameter is determined by device characterization but is not production tested.

3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V. Military, Industrial and Commercial Temperature Ranges

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Тур.	Мах.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V⊪	Input High Voltage	2.2	_	6.0 ⁽²⁾	V
Vi∟	Input Low Voltage	-0.5 ⁽¹⁾		0.8	V

NOTES:

1. VIL (min.) \geq -1.5V for pulse width less than 10ns.

2. VTERM must not exceed Vcc + 10%.

Recommended Operating Temperature and Supply Voltage^(1,2)

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V <u>+</u> 10%
Commercial	0°C to +70°C	0V	5.0V <u>+</u> 10%
Industrial	-40°C to +85°C	0V	5.0V <u>+</u> 10%
			2689 tbl 03

NOTES:

1. This is the parameter TA. This is the "instant on" case temperature.

2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Vcc = 5.0V ± 10%)

			7130SA 7140SA		7130LA 7140LA		
Symbol	Parameter	Test Conditions	Min.	Max.	Min.	Max.	Unit
u	Input Leakage Current ⁽¹⁾	Vcc = 5.5V, VIN = 0V to Vcc	-	10	-	5	μA
llo	Output Leakage Current ⁽¹⁾	Vcc - 5.5V, CE = V⊮, Vou⊤ = 0V to Vcc	_	10	-	5	μA
Vol	Output Low Voltage (I/Oo-I/O7)	Iol = 4mA	-	0.4	_	0.4	V
Vol	Open Drain O <u>utput</u> Low Voltage (BUSY, INT)	lol = 16mA		0.5	1	0.5	V
Vон	Output High Voltage	Юн = -4mA	2.4	1	2.4		V

2689 tbl 04

NOTE:

1. At Vcc < 2.0V leakages are undefined.

2689 tbl 02

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(1,5,7) (Vcc = 5.0V ± 10%)

					7140	X20 ⁽²⁾ X20 ⁽²⁾ I Only	714 Con	0X25 0X25 n'l & itary	7140 Com)X35)X35 h'l& tary	
Symbol	Param eter	Test Condition	Versi	ion	Typ.	Max.	Typ.	Max.	Typ.	Max.	Unit
Icc	Dynamic Operating Current (Both Ports Active)	CEL and CER = VIL, Outputs Disabled f = fMAX ⁽³⁾	COM'L	S A LA	110 110	250 200	110 110	220 170	110 110	165 120	m A
	(Both Pons Active)	1 = IMAX**	MIL & IND	S A LA			110 110	280 220	110 110	230 170	
Isb1	Standby Current (Both Ports - TTL	\overline{CE}_{I} and $\overline{CE}_{R} = V_{IH}$ f = fMAX ⁽³⁾	COM'L	S A LA	30 30	65 45	30 30	65 45	25 25	65 45	m A
	Level Inputs)		MIL & IND	S A LA			30 30	80 60	25 25	80 60	
ISB2	Standby Current (One Port - TTL	$\overline{CE}_{B^*} = V_{IL}$ and $\overline{CE}_{B^*} = V_{IH}^{(6)}$ Active Port OutputsDisabled,	COM'L	S A L A	65 65	165 125	65 65	150 115	50 50	125 90	m A
	Level Inputs)	f=fmax ⁽³⁾	MIL & IND	S A L A			65 65	160 125	50 50	150 115	
Isb3	Full Standby Current (Both Ports - CMOS Level Inputs)	$\frac{\overline{CE}}{\overline{CER}} and \\ \frac{\overline{CER}}{\overline{CER}} \ge V_{CC} - 0.2V, \\ \frac{1}{\sqrt{2}} V_{CC} - 0.2V$	COM'L	S A L A	1.0 0.2	15 5	1.0 0.2	15 5	1.0 0.2	15 4	m A
	CMOS Level inpuis)	$ \begin{array}{l} V_{IN} \geq V cc \ - \ 0.2 V \ or \\ V_{IN} \leq 0.2 V, \ f = 0^{(4)} \end{array} $	MIL & IND	S A L A			1.0 0.2	30 10	1.0 0.2	30 10	
ISB4	Full Standby Current (One Port -	$\frac{\overline{CE}^{*}A^{*}}{\overline{CE}^{*}B^{*}} \stackrel{\leq}{\geq} VCC - 0.2V^{(6)}$	COM'L	S A L A	60 60	155 115	60 60	145 105	45 45	110 85	m A
	ĊMOS Level Inputs)	$V_{IN} \ge \overline{V}_{CC} - 0.2V$ or $V_{IN} \le 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(G)}$	MIL & IND	S A LA		_	60 60	155 115	45 45	145 105	
	•	•			-	-		-		26	589 tbl 06a
					1						—

					714 Com)X55)X55 'I, Ind litary	7140 Com	X100 X100 I, Ind litary	
Symbol	Parameter	Test Condition	Versi	on	Тур.	Max.	Тур.	Max.	Unit
lcc	Dynamic Operating Current (Roth Ports Activo)	\overline{CE}_{L} and $\overline{CE}_{R} = V_{IL}$, Outputs Disabled	COM'L	S A L A	110 110	155 110	110 110	155 110	m A
	(Both Ports Active) $f = f_{MAX}^{(3)}$	MIL & IND	S A LA	110 110	190 140	110 110	190 140		
Isb1	Standby Current (Both Ports - TTL	Ports - TTL $f = fMAX^{(3)}$	COM'L	S A LA	20 20	65 35	20 20	55 35	m A
	Level Inputs)		MIL & IND	S A LA	20 20	65 45	20 20	65 45	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{A^*} = V_{IL}$ and $\overline{CE}_{B^*} = V_{IH}^{(6)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$	COM'L	S A LA	40 40	110 75	40 40	110 75	m A
	Level inputs)	I=IMAX**	MIL & IND	S A LA	40 40	125 90	40 40	125 90	
ISB 3	Full Standby Current (Both Ports -	$\frac{CE_{L}}{CE_{R}} \ge V_{CC} - 0.2V,$	COM'L	S A LA	1.0 0.2	15 4	1.0 0.2	15 4	m A
	CMOS Level Inputs) $V_{IN} \ge V_{CC} - 0.2V_{OT}$ $V_{IN} \le 0.2V$, f = 0 ⁽⁴⁾	$ \begin{array}{l} \forall \mathbb{N} \geq \mathbb{V} \mathbb{CC} \cdot 0.2 \mathbb{V} 0 f \\ \forall \mathbb{N} \leq 0.2 \mathbb{V} f = 0^{ (6)} \end{array} $	MIL & IND	S A LA	1.0 0.2	30 10	1.0 0.2	30 10	
ISB4	Full Standby Current (One Port -	$\overline{CE}^{*}A^{*} \leq 0.2V$ and $\overline{CE}^{*}B^{*} \geq VCC - 0.2V^{(6)}$	COM'L	S A LA	40 40	100 70	40 40	95 70	m A
	CMOS Level Inputs)	$V_{IN} \ge V_{CC} - 0.2V$ or $V_{IN} \le 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(G)}$	MIL & IND	S A L A	40 40	110 85	40 40	110 80	

NOTES:

1. 'X' in part numbers indicates power rating (SA or LA).

2. PLCC and TQFP packages only.

3. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/tcvc, and using "AC TEST CONDITIONS" of input levels of GND to 3V.

5

4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.

5. Vcc = 5V, Ta=+25°C for Typ and is not production tested. Vcc DC = 100 mA (Typ)

6. Port "A" may be either left or right port. Port "B" is opposite from port "A".

7. Industrial temperature: for other speeds, packages and powers contact your sales office.

2689 tb106b

Military, Industrial and Commercial Temperature Ranges

Data Retention Characteristics (LA Version Only)

				7130LA/7140LA			
Symbol	Parameter	Test Condition		Min.	Тур.(1)	Мах.	Unit
Vdr	Vcc for Data Retention			2.0	-	_	V
ICCDR	Data Retention Current		MIL. & IND.	_	100	4000	μA
		Vcc = 2.0V, $\overline{CE} \ge$ Vcc -0.2V	COM'L.		100	1500	
tCDR ⁽³⁾	Chip Deselect to Data Retention Time	$V{\ensuremath{\mathbb N}} \ge V{\ensuremath{\mathbb C}} c$ -0.2V or $V{\ensuremath{\mathbb N}} \le 0.2V$		0	_	_	ns
tr ⁽³⁾	Operation Recovery Time			trc ⁽²⁾	_	_	ns
						2	689 tbl 07

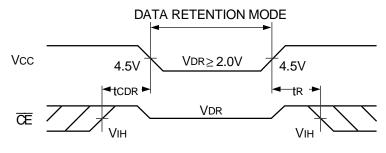
NOTES:

1. Vcc = 2V, TA = $+25^{\circ}$ C, and is not production tested.

2. tRc = Read Cycle Time

3. This parameter is guaranteed but not production tested.

Data Retention Waveform

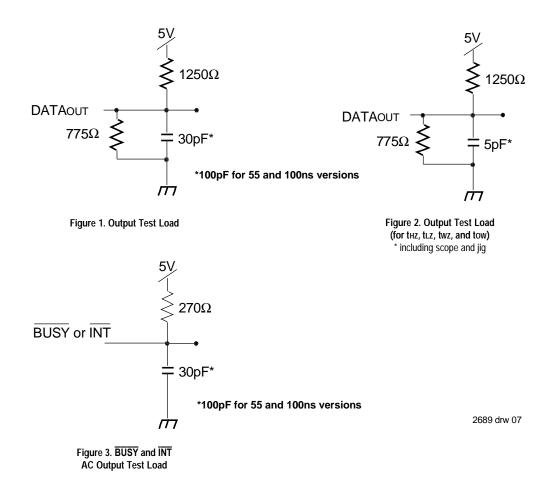


2692 drw 06

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

2689 tbl 08



AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range^(3,5)

		7130X20 ⁽²⁾ 7140X20 ⁽²⁾ 7140X20 ⁽²⁾ 7140X25 Com'l Only Military		7130X35 7140X35 Com'l & Military				
Symbol	Parameter	Min.	Мах.	Min.	Мах.	Min.	Max.	Unit
READ CYCLE						-	-	
trc	Read Cycle Time	20		25	_	35		ns
taa	Address Access Time		20		25		35	ns
tace	Chip Enable Access Time		20		25		35	ns
taoe	Output Enable Access Time	_	11	_	12		20	ns
toн	Output Hold from Address Change	3	_	3		3	_	ns
tLZ	Output Low-Z Time ^(1,4)	0	_	0		0		ns
tHZ	Output High-Z Time ^(1,4)		10		10	_	15	ns
tPU	Chip Enable to Power Up Time ⁽⁴⁾	0		0		0		ns
tpd	Chip Disable to Power Down Time ⁽⁴⁾		20		25		35	ns

)X55)X55 'I, Ind litary	7130X100 7140X100 Com'l, Ind & Military		
Symbol	Parameter	Min. Max.		Min.	Мах.	Unit
READ CYCLE						
tRC	Read Cycle Time	55		100		ns
taa	Address Access Time	_	55		100	ns
tace	Chip Enable Access Time		55		100	ns
taoe	Output Enable Access Time		25		40	ns
toн	Output Hold from Address Change	3	_	10		ns
tLZ	Output Low-Z Time ^(1,4)	5		5	_	ns
tнz	Output High-Z Time ^(1,4)		25		40	ns
tpu	Chip Enable to Power Up Time ⁽⁴⁾	0		0		ns
tpd	Chip Disable to Power Down Time ⁽⁴⁾	_	50		50	ns

2689 tbl 09b

2689 tbl 09a

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage Output Test Load (Figure 2).

2. PLCC, TQFP and STQFP packages only.

3. 'X' in part numbers indicates power rating (SA or LA).

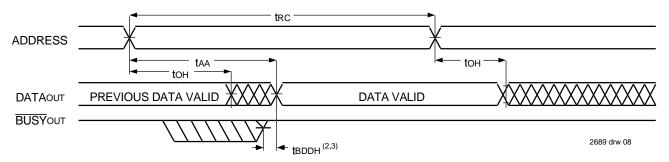
4. This parameter is guaranteed by device characterization, but is not production tested.

5. Industrial temperature: for other speeds, packages and powers contact your sales office.

IDT7130SA/LA and IDT7140SA/LA	
High-Speed 1K x 8 Dual-Port Statio	SR/

Timing Waveform of Read Cycle No. 1, Either Side⁽¹⁾

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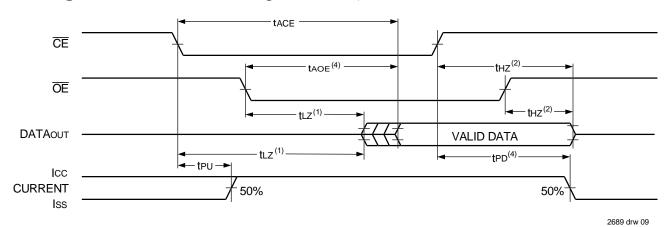


NOTES:

1. $R/\overline{W} = V_{H}, \overline{CE} = V_{L}$, and is $\overline{OE} = V_{L}$. Address is valid prior to the coincidental with \overline{CE} transition LOW.

2. tedd delay is required only in the case where the opposite port is completing a write operation to the same the address location. For simultaneous read operations, BUSY has no relationship to valid output data.

3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.



Timing Waveform of Read Cycle No. 2, Either Side⁽³⁾

- 1. Timing depends on which signal is asserted last, \overline{OE} or \overline{CE} .
- 2. Timing depends on which signal is deaserted first, \overline{OE} or \overline{CE} .
- 3. $R/\overline{W} = V_{H}$ and $\overline{OE} = V_{IL}$, and the address is valid prior to or coincidental with \overline{CE} transition LOW.
- 4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range^(5,6)

		7130X20 ^{¢)} 7140X20 ^{¢)} Com'l Only		7130X25 7140X25 Com'l & Military		7130X35 7140X35 Com'l & Military			
Symbol	Parameter	Min.	Мах.	Min.	Мах.	Min.	Мах.	Unit	
WRITE CYCLE									
twc	Write Cycle $Time^{(\!\!\!\mathfrak{S})}$	20		25		35		ns	
tew	Chip Enable to End-of-Write	15		20	_	30	_	ns	
taw	Address Valid to End-of-Write	15		20		30		ns	
tas	Address Set-up Time	0		0	-	0	-	ns	
twp	Write Pulse Width ⁽⁴⁾	15		15		25		ns	
twr	Write Recovery Time	0		0	_	0	_	ns	
tow	Data Valid to End-of-Write	10		12		15	_	ns	
tHZ	Output High-Z Time ⁽¹⁾		10	_	10		15	ns	
tdн	Data Hold Time	0		0	-	0	_	ns	
twz	Write Enable to Output in High-Z ⁽¹⁾		10	_	10		15	ns	
tow	Output Active from End-of-Write ⁽¹⁾	0		0		0		ns	
	·	•	•	•			•	2689 tbl 10	
				714	0X55 0X55 'l, Ind	7140)X100)X100 'I, Ind		

		7140X55 Com'l, Ind & Military		7140X100 Com'l, Ind & Military			
Symbol	Parameter	Min. Max.		Min. Max.		Unit	
WRITE CYCL	E						
twc	Write Cycle Time ⁽³⁾	55	_	100		ns	
tew	Chip Enable to End-of-Write	40		90		ns	
taw	Address Valid to End-of-Write	40	_	90		ns	
tas	Address Set-up Time	0	_	0		ns	
twp	Write Pulse Width ⁽⁴⁾	30	_	55		ns	
twr	Write Recovery Time	0	_	0		ns	
tow	Data Valid to End-of-Write	20		40		ns	
tHZ	Output High-Z Time ⁽¹⁾		25		40	ns	
tDH	Data Hold Time	0		0		ns	
twz	Write Enable to Output in High-Z ⁽¹⁾		25		40	ns	
tow	Output Active from End-of-Write ⁽¹⁾	0	_	0		ns	
		-	-	•	-	2689 tbl 10b	

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.

2. PLCC, TQFP and STQFP packages only.

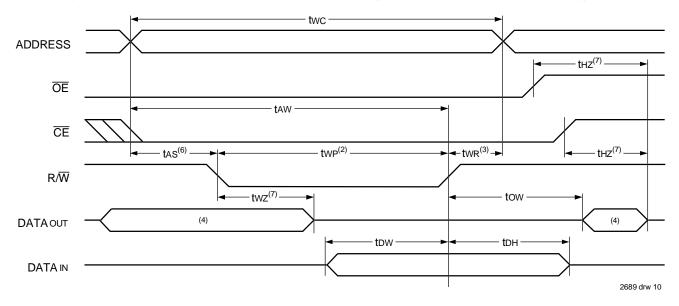
5. 'X' in part numbers indicates power rating (SA or LA).

6. Industrial temperature: for other speeds, packages and powers contact your sales office.

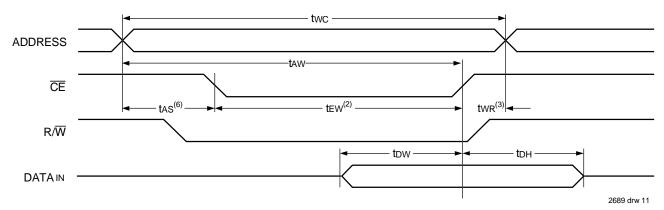
^{3.} For MASTER/SLAVE combination, two = tBAA + twp, since R/W = VIL must occur after tBAA.

^{4.} If \overline{OE} is LOW during a R \overline{W} controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off data to be placed on the bus for the required tow. If \overline{OE} is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

Timing Waveform of Write Cycle No. 1, (R/W Controlled Timing)^(1,5,8)



Timing Waveform of Write Cycle No. 2, (CE Controlled Timing)^(1,5)



- 1. R/\overline{W} or \overline{CE} must be HIGH during all address transitions.
- 2. A write occurs during the overlap (tew or twp) of $\overline{CE} = VIL$ and $R/\overline{W} = VIL$.
- 3. two is measured from the earlier of \overline{CE} or R/W going HIGH to the end of the write cycle.
- 4. During this period, the I/O pins are in the output state and input signals must not be applied.
- 5. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in the HIGH impedance state.
- 6. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is asserted last.
- 7. This parameter is determined be device characterization, but is not production tested. Transition is measured 0mV from steady state with the Output Test Load (Figure 2).
- If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of twp or (twz + tow) to allow the I/O drivers to turn off data to be placed on the bus for the required tow. If OE is HIGH during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified twp.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(7,9)

		713 714 Com'	714 Cor	0X25 0X25 n'l & itary	7130X35 7140X35 Com'l & Military			
Symbol	Parameter	Min.	Мах.	Min.	Мах.	Min.	Мах.	Unit
BUSY TIMING	(For MASTER IDT 7130)			-				
tbaa	BUSY Access Time from Address		20	—	20		20	ns
tBDA	BUSY Disable Time from Address		20	—	20		20	ns
tbac	BUSY Access Time from Chip Enable		20	—	20		20	ns
tBDC	BUSY Disable Time from Chip Enable	—	20	—	20		20	ns
twн	Write Hold After BUSY ⁽⁶⁾	12		15	_	20		ns
twdd	Write Pulse to Data Delay ⁽²⁾		40	_	50		60	ns
todd	Write Data Valid to Read Data Delay ⁽²⁾		30	_	35		35	ns
taps	Arbitration Priority Set-up Time ⁽³⁾	5		5	_	5	_	ns
tBDD	BUSY Disable to Valid Data ⁽⁴⁾		25	-	35		35	ns
BUSY INPUT	TIMING (For SLAVE IDT 7140)							
twв	Write to BUSY Input ⁽⁵⁾	0		0	_	0		ns
twн	Write Hold After BUSY ⁽⁶⁾	12		15	_	20		ns
twdd	Write Pulse to Data Delay ⁽²⁾		40	_	50		60	ns
todd	Write Data Valid to Read Data Delay ⁽²⁾		30		35		35	ns
	·			I	I	1		2689 tbl 11 a
			1	714 Com	0X55 0X55 11, Ind ilitary	7140 Com)X100)X100 'I, Ind ilitary	2689 tbl 11 a
Symbol	Parameter		1	714 Com	0X55 ı'l, Ind	7140 Com)X100)X100 'I, Ind	2689 tbl 11 a Unit
	Parameter ; (For MASTER IDT 7130)		1	714 Com & M	0X55 I'l, Ind ilitary	7140 Com & Mi)X100)X100 'I, Ind ilitary	
			I	714 Com & M	0X55 I'l, Ind ilitary	7140 Com & Mi)X100)X100 'I, Ind ilitary	
BUSY TIMING	(For MASTER IDT 7130)			714 Com & M Min.	0X55 i'l, Ind ilitary Max.	714(Com & Mi Min.	0X100 0X100 'I, Ind ilitary Max.	Unit
BUSY TIMING	6 (For MASTER IDT 7130) BUSY Access Time from Address]			714 Com & M Min.	0X55 i'l, Ind ilitary Max. 30	714(Com & Mi Min.	0X100 0X100 1, Ind litary Max. 50	Unit ns
BUSY TIMING tBAA tBDA	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address			714 Com & M Min.	0X55 i'l, Ind ilitary Max. 30 30	714(Com & Mi Min.	0X100 0X100 'I, Ind ilitary Max. 50 50	Unit ns ns
BUSY TIMING tBAA tBDA tBAC	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable			714 Com & M Min.	0X55 i'l, Ind ilitary Max. 30 30 30	7140 Com & Mi Min.	0X100 0X100 11, Ind 11itary Max. 50 50 50	Unit ns ns
BUSY TIMING tBAA tBDA tBAC tBDC	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable BUSY Disable Time from Chip Enable			714 Com & M Min.	0X55 '1, Ind ilitary Max. 30 30 30 30 30	7140 Com & Mi Min.	X100 X100 'I, Ind litary 50 50 50 50	Unit ns ns ns ns
BUSY TIMING tBAA tBDA tBAC tBDC tWH	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable BUSY Disable Time from Chip Enable Write Hold After BUSY ⁽⁶⁾			714 Com & M Min. — — — — 20	0X55 1, Ind ilitary Max. 30 30 30 30 30 	714(Com & Min. — — — — 20	X100 X100 'I, Ind litary Max. 50 50 50 50 	Unit ns ns ns ns
BUSY TIMING IBAA IBDA IBAC IBDC tWH twDD	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable BUSY Disable Time from Chip Enable Write Hold After BUSY ⁽⁶⁾ Write Pulse to Data Delay ⁽²⁾			714 Com & M Min. — — — — 20	0X55 '1, Ind ilitary Max. 30 30 30 30 30 30 80	714(Com & Min. — — — — 20	X100 X100 Y1, Ind litary 50 50 50 50 50 120	Unit ns ns ns ns ns ns
BUSY TIMING tBAA tBDA tBAC tBDC tWH tWDD tDDD	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable BUSY Disable Time from Chip Enable Write Hold After BUSY ⁽⁶⁾ Write Pulse to Data Delay ⁽²⁾ Write Data Valid to Read Data Delay ⁽²⁾			714 Com & M Min. — — — — 20 — — 20	0X55 1, Ind ilitary Max. 30 30 30 30 30 30 80 55	714(Com & Min. — — — — 20 — —	X100 X100 'I, Ind liitary 50 50 50 50 	Unit ns ns ns ns ns ns ns ns
BUSY TIMING IBAA IBDA IBDA IBAC IBDC IBDC IWH IWDD ICDD IAPS IBDD	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable BUSY Disable Time from Chip Enable Write Hold After BUSY ⁽⁶⁾ Write Pulse to Data Delay ⁽²⁾ Write Data Valid to Read Data Delay ⁽²⁾ Arbitration Priority Set-up Time ⁽³⁾			714 Com & M Min. — — — — 20 — — 20	0X55 '1, Ind ilitary Max. 30 30 30 30 30 30 30 30 55 55 	714(Com & Min. — — — — 20 — —	X100 X100 Y1, Ind liitary Max. 50 50 50 50 50 120 100 	Unit ns ns ns ns ns ns ns ns ns
BUSY TIMING IBAA IBDA IBDA IBDC IBDC IWH IWDD ICDD IAPS IBDD	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable BUSY Disable Time from Chip Enable Write Hold After BUSY ⁽⁶⁾ Write Pulse to Data Delay ⁽²⁾ Write Data Valid to Read Data Delay ⁽²⁾ Arbitration Priority Set-up Time ⁽³⁾ BUSY Disable to Valid Data ⁽⁴⁾			714 Com & M Min. — — — — 20 — — 20	0X55 '1, Ind ilitary Max. 30 30 30 30 30 30 30 30 55 55 	714(Com & Min. — — — — 20 — —	X100 X100 Y1, Ind liitary Max. 50 50 50 50 50 120 100 	Unit ns ns ns ns ns ns ns ns ns
BUSY TIMING IBAA IBDA IBDA IBDC IBDC IWH IWDD IDDD IAPS IBDD BUSY INPUT	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable BUSY Disable Time from Chip Enable Write Hold After BUSY ⁽⁶⁾ Write Pulse to Data Delay ⁽²⁾ Write Data Valid to Read Data Delay ⁽²⁾ Arbitration Priority Set-up Time ⁽³⁾ BUSY Disable to Valid Data ⁽⁴⁾			714 Com & M Min. 	0X55 'I, Ind ilitary Max. 30 30 30 30 30 30 30 55 55	714(Com & Min. — — — 20 — 20 — 5 —	X100 X100 Y1, Ind litary 50 50 50 50 50 120 100 65	Unit ns ns ns ns ns ns ns ns ns ns
BUSY TIMING IBAA IBDA IBDA IBDC IBDC IBDC IWH IWDD IDDD IDDD IDDD IBDD IBDSY INPUT IWB	For MASTER IDT 7130) BUSY Access Time from Address] BUSY Disable Time from Address BUSY Access Time from Chip Enable BUSY Disable Time from Chip Enable Write Hold After BUSY ⁽⁶⁾ Write Pulse to Data Delay ⁽²⁾ Write Data Valid to Read Data Delay ⁽²⁾ Arbitration Priority Set-up Time ⁽³⁾ BUSY Disable to Valid Data ⁽⁴⁾ TIMING (For SLAVE IDT 7140) Write to BUSY Input ⁽⁵⁾			714 Com & M Min. 	0X55 'I, Ind ilitary Max. 30 30 30 30 30 30 30 55 55 	714C Com & Min. 	X100 X100 Y1, Ind liitary 50 50 50 50 50 120 120 100 65	Unit ns ns ns ns ns ns ns ns ns ns

NOTES:

1. PLCC, TQFP and STQFP packages only.

2. Port-to-port delay through RAM cells from the writing port to the reading port, refer to "Timing Waveform of Write with Port -to-Port Read and BUSY."

3. To ensure that the earlier of the two ports wins.

4. tBDD is a calculated parameter and is the greater of 0, twDD - twp (actual) or tDDD - tDw (actual).

5. To ensure that a write cycle is inhibited on port 'B' during contention on port 'A'.

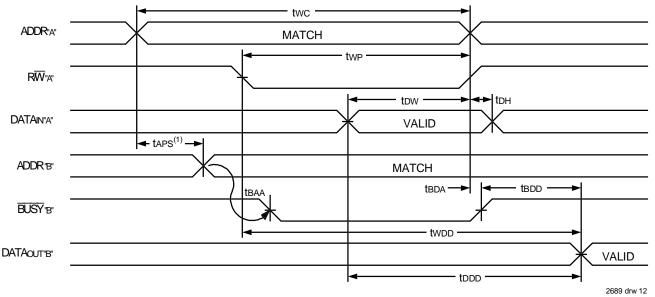
6. To ensure that a write cycle is completed on port 'B' after contention on port 'A'.

7. 'X' in part numbers indicates power rating (S or L).

8. Industrial temperature: for other speeds, packages and powers contact your sales office.

2689 tbl 11b

Timing Waveform of Write with Port-to-Port Read and BUSY^(2,3,4)



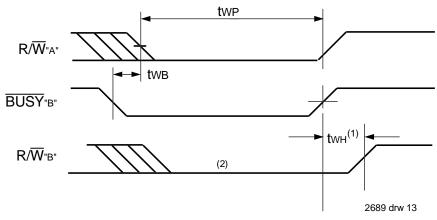
NOTES:

1. To ensure that the earlier of the two ports wins. tBDD is ignored for slave (IDT7140).

- 2. $\overline{CE}L = \overline{CE}R = VIL$
- 3. $\overline{OE} = V_{IL}$ for the reading port.

4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port "B" is opposite from port "A".

Timing Waveform of Write with $\overline{\text{BUSY}}^{(3)}$



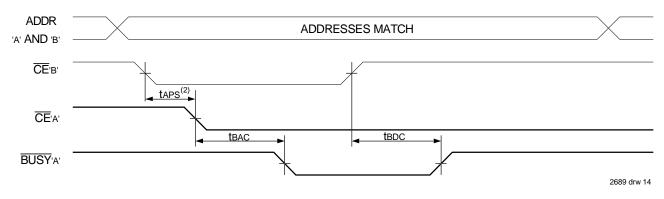
NOTES:

1. twH must be met for both BUSY Input (IDT7140, slave) or Output (IDT7130 master).

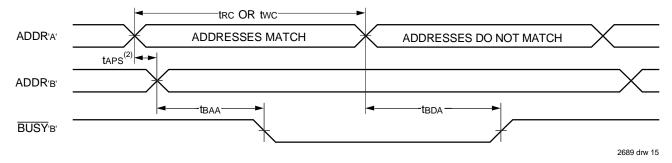
2. BUSY is asserted on port "B" blocking R/W"B", until BUSY"B" goes HIGH.

3. All timing is the same for the left and right ports. Port "A" may be either the left or right port. Port "B" is oppsite from port "A".

Timing Waveform of $\overline{\text{BUSY}}$ Arbitration Controlled by $\overline{\text{CE}}$ Timing⁽¹⁾



Timing Waveform by **BUSY** Arbitration Controlled by Address Match Timing⁽¹⁾



NOTES:

1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

2. If taps is not satisified, the BUSY will be asserted on one side or the other, but there is no guarantee on which side BUSY will be asserted (7130 only).

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range^(2,3)

•		7140	X20 ⁽¹⁾ X20 ⁽¹⁾ I Only	7130X25 7140X25 Com'l &		7130X35 7140X35 Com'l &		
Symbol	Parameter	Min. Max.		Mili Min.	tary Max.	Mil Min.	itary Max.	Unit
INTERRUPT	TIMING			1		l		J
tas	Address Set-up Time	0		0		0	—	ns
twr	Write Recovery Time	0	_	0		0	—	ns
ti∾s	Interrupt Set Time		20		25		25	ns
tinr	Interrupt Reset Time		20		25		25	ns
	•	-	-	_		_	-	- 2689 tbl 12

NOTES:

1. PLCC, TQFP and STQFP package only.

2. 'X' in part numbers indicates power rating (SA or LA).

3. Industrial temperature: for other speeds, packages and powers contact your sales office.

AC Electrical characteristics Over the Operating Temperature and Supply Voltage Range^(1,2)

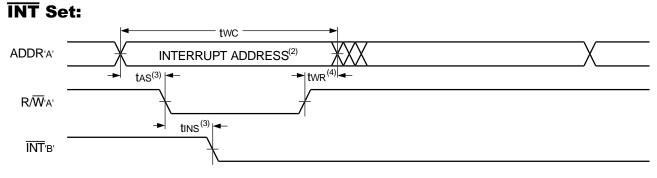
		714 Com	0X55 0X55 1, Ind litary	7130X100 7140X100 Com'l, Ind & Military		
Symbol	Parameter	Min.	Max.	Unit		
INTERRUPT	TIMING					
tas	Address Set-up Time	0		0		ns
twr	Write Recovery Time	0		0		ns
tiNS	Interrupt Set Time		45		60	ns
tinr	Interrupt Reset Time		45		60	ns

NOTES:

1. 'X' in part numbers indicates power rating (SA or LA).

2. Industrial temperature: for other speeds, packages and powers contact your sales office.

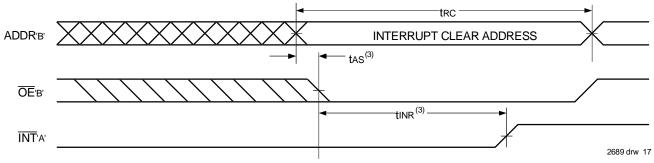
Timing Waveform of Interrupt Mode⁽¹⁾



2689 drw 16

2689 tbl 12b

INT Clear:



- 1. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- 2. See Interrupt Truth Table II.
- 3. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is asserted last.
- 4. Timing depends on which enable signal (CE or R/W) is de-asserted first.

Truth Tables

Truth Table I — Non-Contention Read/Write Control⁽⁴⁾

Inputs ⁽¹⁾				
R/₩	Ē	ŌĒ	D0-7	Function
Х	Н	Х	Z	Port Disabled and in Power-Down Mode, IsB2 or IsB4
Х	Н	Х	Z	$\overline{CER} = \overline{CEL} = VH$, Power-Down Mode, ISB1 or ISB3
L	L	Х	DATAIN	Data on Port Written into Memory [©]
Н	L	L	DATAOUT	Data in Memory Output on Port ⁽³⁾
Н	L	Н	Z	High Impedance Outputs

NOTES:

1. AOL – A10L • AOR – A10R.

2. If $\overline{\text{BUSY}}$ = L, data is not written.

3. If $\overline{\text{BUSY}} = L$, data may not be valid, see twod and todd timing.

4. 'H' = VIH, 'L' = VIL, 'X' = DON'T CARE, 'Z' = HIGH IMPEDANCE

Truth Table II — Interrupt Flag^(1,4)

Left Port				Right Port						
R/₩L	CEL	ŌĒL	A9L-A0L	ĪNTL	R/WR		ŌĒR	A9R-A0R	INT _R	Function
L	L	Х	3FF	Х	Х	Х	Х	Х	L ⁽²⁾	Set Right INTR Flag
х	Х	Х	Х	Х	Х	L	L	3FF	H ⁽³⁾	Reset Right INTR Flag
Х	Х	Х	Х	L ⁽³⁾	L	L	Х	3FE	Х	Set Left INT∟ Flag
Х	L	L	3FE	H ⁽²⁾	Х	Х	Х	Х	Х	Reset Left INTL Flag

NOTES:

1. Assumes $\overline{\text{BUSY}}$ L = $\overline{\text{BUSY}}$ R = VIH

2. If $\overline{\text{BUSY}}$ L = VIL, then No Change.

3. If $\overline{\text{BUSY}}R = \text{VIL}$, then No Change.

4. 'H' = HIGH,' L' = LOW,' X' = DON'T CARE

Truth Table III — Address **BUSY** Arbitration

Inputs			Out	puts	
ĒĒ∟	CE _R	Aol-A9l Aor-A9r	BUSYL ⁽¹⁾	BUSY _R ⁽¹⁾	Function
Х	Х	NO MATCH	Н	Н	Normal
Н	Х	MATCH	Н	Н	Normal
Х	Н	MATCH	Н	Н	Normal
L	L	MATCH	(2)	(2)	Write Inhibit ⁽³⁾

NOTES:

2689 tbl 15

- Pins BUSY_L and BUSY_R are both outputs for IDT7130 (master). Both are inputs for IDT7140 (slave). BUSY_X outputs on the IDT7130 are open drain, not push-pull outputs. On slaves the BUSY_X input internally inhibits writes.
- 2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If tAPS is not met, either $\overline{\text{BUSY}}_{\text{L}}$ or $\overline{\text{BUSY}}_{\text{R}}$ = LOW will result. $\overline{\text{BUSY}}_{\text{L}}$ and $\overline{\text{BUSY}}_{\text{R}}$ outputs can not be LOW simultaneously.
- Writes to the left port are internally ignored when BUSYL outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when BUSYR outputs are driving LOW regardless of actual logic level on the pin.

2689 tbl 14

2689 tbl 13

Functional Description

The IDT7130/IDT7140 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7130/IDT7140 has an automatic power down feature controlled by \overline{CE} . The \overline{CE} controls onchip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE} = VIH$). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (\overline{INTL}) is asserted when the right port writes to memory location 3FE (HEX), where a write is defined as the $\overline{CER} = R/\overline{WR} = VIL$ per Truth Table II. The left port clears the interrupt by access address location 3FE access when $\overline{CEL} = \overline{OEL} = VIL$, R/W is a "don't care". Likewise, the right port interrupt flag (\overline{INTR}) is asserted when the left port writes to memory location 3FF (HEX) and to clear the interrupt flag (\overline{INTR}), the right port must access the memory location 3FF. The message (8 bits) at 3FE or 3FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 3FE and 3FF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table II for the interrupt operation.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "Busy". The $\overline{\text{BUSY}}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{\text{BUSY}}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of BUSY logic is not required or desirable for all applications. In some cases it may be useful to logically OR the BUSY outputs together and use any BUSY indication as an interrupt source to flag the event of an illegal or illogical operation. In slave mode the BUSY pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the BUSY pins HIGH. If desired, unintended write operations can be prevented to a port by tying the BUSY pin for that port LOW.

The BUSY outputs on the IDT7130 RAM (Master) are open drain type outputs and require open drain resistors to operate. If these

Military, Industrial and Commercial Temperature Ranges

RAMs are being expanded in depth, then the BUSY indication for the resulting array does not require the use of an external AND gate.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an RAM array in width while using busy logic, one master part is used to decide which side of the RAM array will receive a busy indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the busy signal as a write inhibit signal. Thus on the IDT7130/IDT7140 RAMs the BUSY pin is an output if the part is Master (IDT7130), and the BUSY pin is an input if the part is a Slave (IDT7140) as shown in Figure 3.

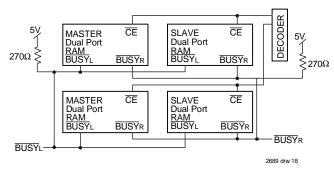
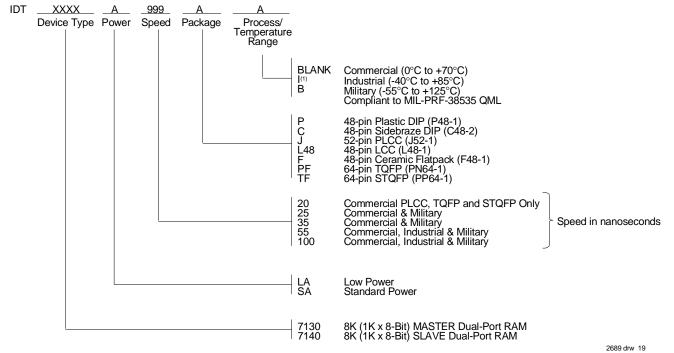


Figure 3. Busy and chip enable routing for both width and depth expansion with IDT7130 (Master) and IDT7140 (Slave)RAMs.

If two or more master parts were used when expanding in width, a split decision could result with one master indicating busy on one side of the array and another master indicating busy on one other side of the array. This would inhibit the write operations from one port for part of a word and inhibit the write operations from the other port for the other part of the word.

The $\overline{\text{BUSY}}$ arbitration, on a Master, is based on the chip enable and address signals only. It ignores whether an access is a read or write. In a master/slave array, both address and chip enable must be valid long enough for a $\overline{\text{BUSY}}$ flag to be output from the master before the actual write pulse can be initiated with either the R/W signal or the byte enables. Failure to observe this timing can result in a glitched internal write inhibit signal and corrupted data in the slave.

Ordering Information



NOTE:

 Industrial temperature range is available on selected PLCC packages in standard temperature. For other speeds, packages and powers contact your sales office.

Datasheet Document History

3/15/99:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Pages 2 and 3 Added additional notes to pin configurations
6/8/99:	Changed drawing format
8/2/99:	Page 2 Corrected package number in note 3
9/29/99:	Page 2 Fixed pin 1 in DIP pin configuration
11/10/99:	Replaced IDT logo
6/23/00:	Page 4 Increased storage temperature parameters
	Clarified TAparameter
	Page 5 DC Electrical parameters-changed wording from "open" to "disabled"
	Changed ±500mV to 0mV in notes



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