OPA2320-Q1 Precision, 20-MHz, 0.9-pA, Low-Noise, RRIO, CMOS Operational Amplifier

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Precision with Zero-Crossover Distortion:
  - Low Offset Voltage: 150 µV (max)
  - High CMRR: 114 dB
  - Rail-to-Rail I/O
- Low Input Bias Current: 0.9 pA (max)
- Low Noise: 7 nV/√Hz at 10kHz
- Wide Bandwidth: 20 MHz
- Slew Rate: 10 V/µs
- Quiescent Current: 1.45 mA/ch
- Single-Supply Voltage Range: 1.8 to 5.5 V
- Unity-Gain Stable
- Small VSSOP Package

2 Applications

- Automotive
- High-Z Sensor Signal Conditioning
- Transimpedance Amplifiers
- Test and Measurement Equipment
- Programmable Logic Controllers (PLCs)
- Motor Control Loops
- Communications
- Input and Output ADC and DAC Buffers
- Active Filters

3 Description

The OPA2320-Q1 device is a new generation of precision low-voltage CMOS operational amplifiers (op amps) optimized for very low noise and wide bandwidth while operating on a low quiescent current of only 1.45 mA.

The OPA2320-Q1 device is ideal for low-power, single-supply applications. Low-noise (7 nV/√Hz) and high-speed operation also makes the device well-suited for driving sampling analog-to-digital converters (ADCs). Other applications include signal conditioning and sensor amplification.

The OPA2320-Q1 device features a linear input stage with zero-crossover distortion that delivers excellent common-mode rejection ratio (CMRR) of 114 dB (typical) over the full input range. The input common-mode range extends 100 mV beyond the negative and positive supply rails. The output voltage typically swings within 10 mV of the rails.

In addition, the OPA2320-Q1 device has a wide supply voltage range from 1.8 to 5.5 V with excellent PSRR (106 dB) over the entire supply range, making the device suitable for precision, low-power applications that run directly from batteries without regulation.

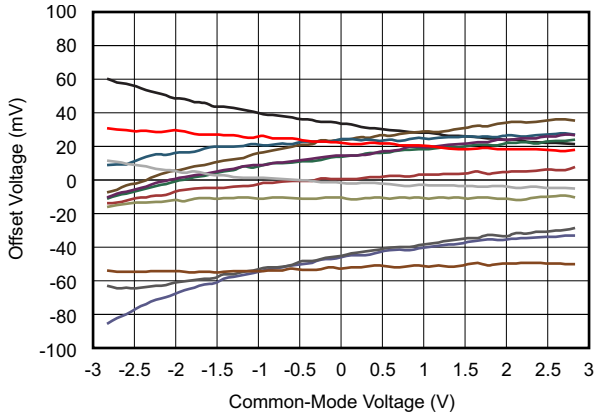
The OPA2320-Q1 device is available in an 8-pin VSSOP (DGK) package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA2320-Q1	VSSOP	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Zero Crossover Distortion: Low Offset Voltage



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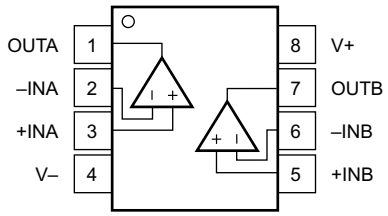
4 Revision History

DATE	REVISION	NOTES
September 2014	*	Initial release.

5 Pin Configuration and Functions

8-Pin VSSOP
DGK Package
Top View



Pin Functions

PIN		DESCRIPTION
NAME	NO.	
–INA	2	Inverting input (channel A)
+INA	3	Non-inverting input (channel A)
–INB	6	Inverting input (channel B)
+INB	5	Non-inverting input (channel B)
OUTA	1	Output (channel A)
OUTB	7	Output (channel B)
V–	4	Negative supply or ground (for single-supply operation)
V+	8	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Supply voltage	V+ and V–		6	V
Voltage(2)	Signal input pins	$V_{(V–)}$ – 0.5	$V_{(V+)}$ + 0.5	V
Current(2)	Signal input pins	–10	10	mA
	Output short-circuit current(3)	Continuous		mA
Operating temperature, T_A		–40	150	°C
Junction temperature, T_J			150	°C

(1) Stresses beyond those listed as *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated as *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5 V beyond the supply rails should be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		–2000	2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	–750	750	
			Other pins	–500	500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_S	Supply voltage	1.8 (±0.9)		5.5 (±2.75)	V
T_A	Ambient operating temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		DGK 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	174.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	95	
ψ_{JT}	Junction-to-top characterization parameter	2	
ψ_{JB}	Junction-to-board characterization parameter	93.5	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics:

V_S = 1.8 to 5.5 V or ±0.9 V to ±2.75 V. At T_A = 25°C, $R_{(L)}$ = 10 kΩ connected to V_S / 2, $V_{(CM)}$ = V_S / 2, V_O = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{IO}	Input offset voltage			40	150	µV
	Input offset voltage versus temperature	V_S = 5.5 V, T_A = –40°C to 125°C		1.5	5	µV/°C
	Input offset voltage versus power supply	V_S = 1.8 to 5.5 V		5	20	µV/V
		V_S = 1.8 to 5.5 V, T_A = –40°C to 125°C		15		
	Input offset-voltage channel separation	At 1 kHz		130		dB
INPUT VOLTAGE						
$V_{(CM)}$	Common-mode voltage range		$V_{(V–)}$ – 0.1		$V_{(V+)}$ + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, $V_{(V–)}$ – 0.1 V < $V_{(CM)}$ < $V_{(V+)}$ + 0.1 V	100	114		dB
	Common-mode rejection ratio, over temperature	V_S = 5.5 V, $V_{(V–)}$ – 0.1 V < $V_{(CM)}$ < $V_{(V+)}$ + 0.1 V, T_A = –40°C to 125°C	96			dB
INPUT BIAS CURRENT						
I_{IB}	Input bias current			±0.2	±0.9	pA
	Input bias current, over temperature	T_A = –40°C to 85°C			±50	pA
		T_A = –40°C to 125°C			±400	pA
I_{IO}	Input offset current			±0.2	±0.9	pA
	Input offset current, over temperature	T_A = –40°C to 85°C			±50	pA
		T_A = –40°C to 125°C			±400	pA
NOISE						
$V_{I(n)}$	Input voltage noise	f = 0.1 to 10 Hz		2.8		μV_{PP}
	Input voltage noise density	f = 1 kHz		8.5		nV/√Hz
		f = 10 kHz		7		nV/√Hz
	Input current noise density	f = 1 kHz		0.6		fA/√Hz
INPUT CAPACITANCE						
	Differential			5		pF
	Common-mode			4		pF
OPEN-LOOP GAIN						
$A_{(OL)}$	Open-loop voltage gain	0.1 V < V_O < $V_{(V+)}$ – 0.1 V, $R_{(L)}$ = 10 kΩ	114	132		dB
		0.1 V < V_O < $V_{(V+)}$ – 0.1 V, $R_{(L)}$ = 10 kΩ, T_A = –40°C to 125°C	100	130		dB
		0.2 V < V_O < $V_{(V+)}$ – 0.2 V, $R_{(L)}$ = 2 kΩ	108	123		dB
		0.2 V < V_O < $V_{(V+)}$ – 0.2 V, $R_{(L)}$ = 2 kΩ, T_A = –40°C to 125°C	96	130		dB
PM	Phase margin	V_S = 5 V, $C_{(L)}$ = 50 pF		47		°
FREQUENCY RESPONSE, V_S = 5 V, $C_{(L)}$ = 50 pF						
GBP	Gain bandwidth product	Unity gain		20		MHz
SR	Slew rate	G = 1		10		V/µs
t_s	Settling time	To 0.1%, 2-V step, G = 1		0.25		µs
		To 0.01%, 2-V step, G = 1		0.32		
		To 0.0015%, 2-V step, G = 1 (1)		0.5		
	Overload recovery time	V_I × G > V_S		100		ns
THD+N	Total harmonic distortion + noise (2)	V_O = 4 V_{PP}, G = 1, f = 10 kHz, $R_{(L)}$ = 10 kΩ		0.0005%		
		V_O = 4 V_{PP}, G = 1, f = 10 kHz, $R_{(L)}$ = 600 kΩ		0.0011%		

(1) Based on simulation.
(2) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: (continued)

V_S = 1.8 to 5.5 V or ±0.9 V to ±2.75 V. At T_A = 25°C, $R_{(L)}$ = 10 kΩ connected to V_S / 2, $V_{(CM)}$ = V_S / 2, V_O = V_S / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
V_O	Voltage output swing from both rails	$R_{(L)}$ = 10 kΩ		10	20	mV
		$R_{(L)}$ = 10 kΩ, T_A = –40°C to 125°C			30	
		$R_{(L)}$ = 2 kΩ		25	35	
		$R_{(L)}$ = 2 kΩ, T_A = –40°C to 125°C			45	
$I_{(SC)}$	Short-circuit current	V_S = 5.5 V		±65		mA
$C_{(L)}$	Capacitive load drive		See Typical Characteristics			
	Open-loop output resistance	I_O = 0 mA, f = 1MHz		90		Ω
POWER SUPPLY						
V_S	Specified voltage range		1.8		5.5	V
I_Q	Quiescent current per amplifier	I_O = 0 mA, V_S = 5.5V		1.45	1.6	mA
		I_O = 0 mA, V_S = 5.5V, T_A = –40°C to 125°C			1.7	
	Power-on time	$V_{(V+)}$ = 0 to 5 V, to 90% I_Q level		28		µs
TEMPERATURE						
	Specified range		–40		125	°C
	Operating range		–40		150	°C

6.6 Typical Characteristics

At T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ, unless otherwise noted.

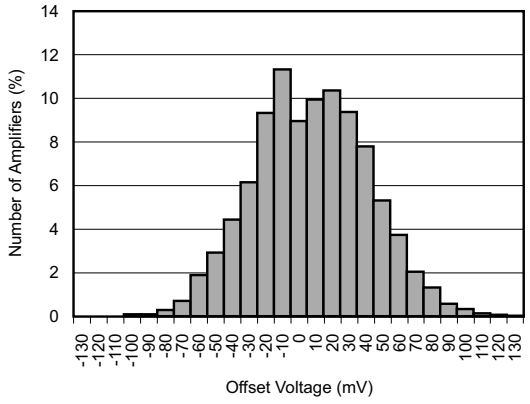


Figure 1. Offset Voltage Production distribution

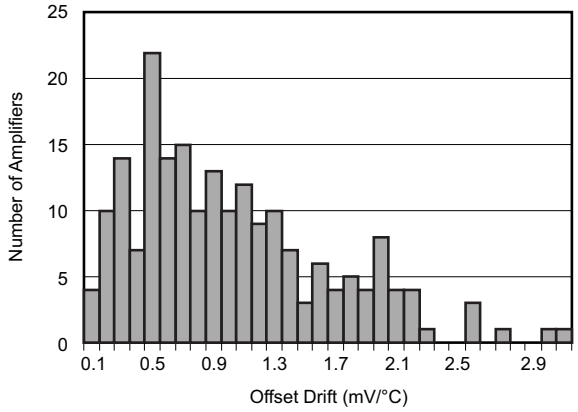


Figure 2. Offset Voltage Drift Distribution

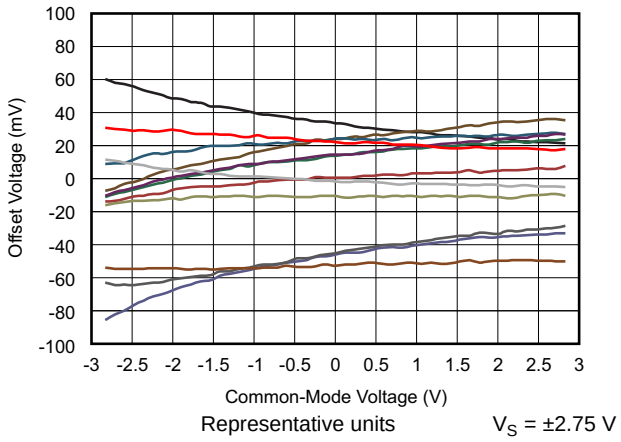


Figure 3. Offset Voltage vs Common-Mode Voltage

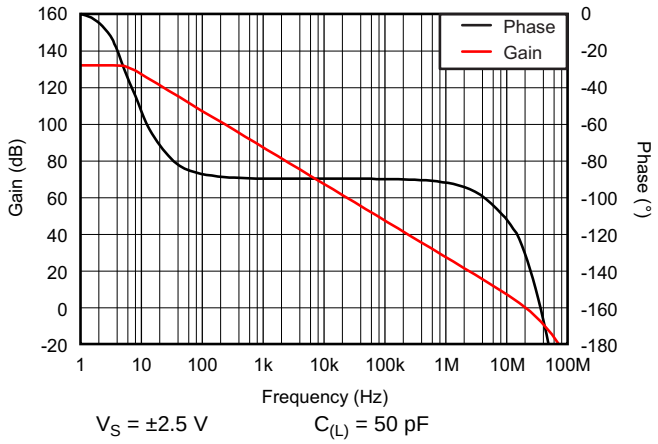


Figure 4. Open-Loop Gain and Phase vs Frequency

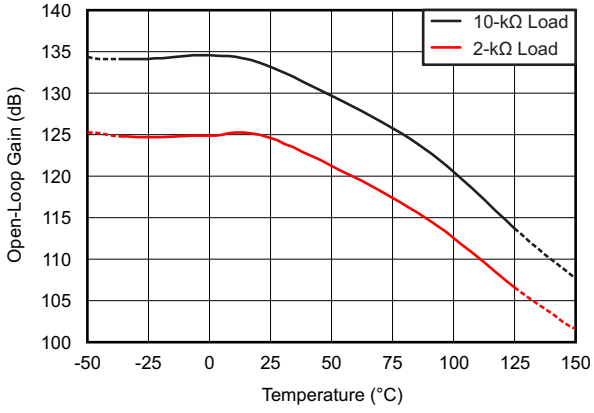


Figure 5. Open-Loop Gain vs Temperature

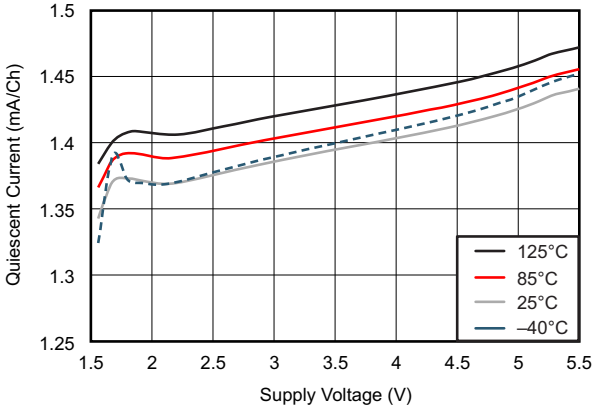


Figure 6. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

At T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ, unless otherwise noted.

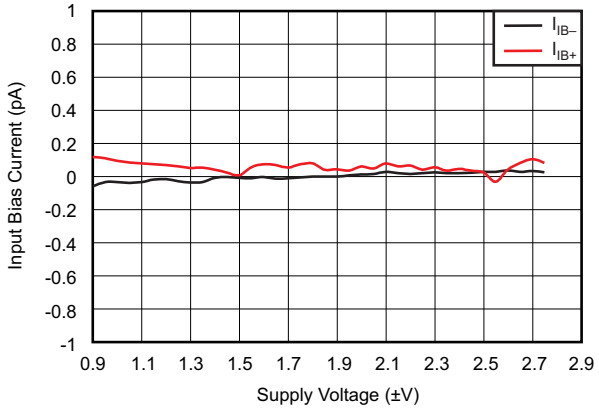


Figure 7. Input Bias Current vs Supply Voltage

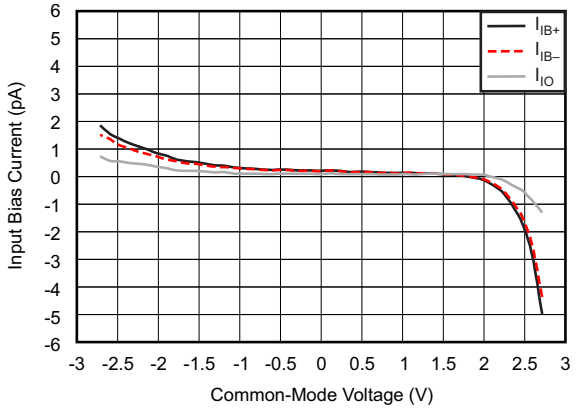


Figure 8. Input Bias Current vs Common-Mode Voltage

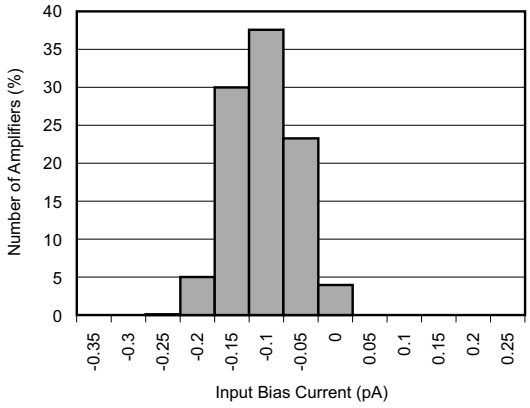


Figure 9. Input Bias Current Distribution

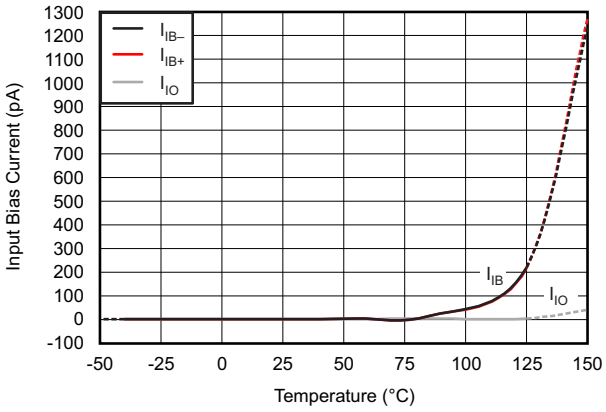


Figure 10. Input Bias Current vs Temperature

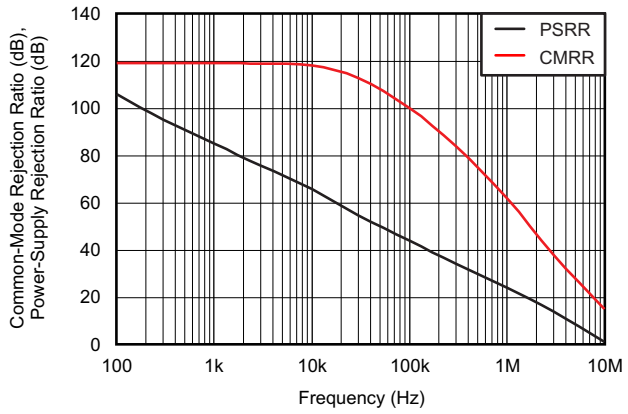
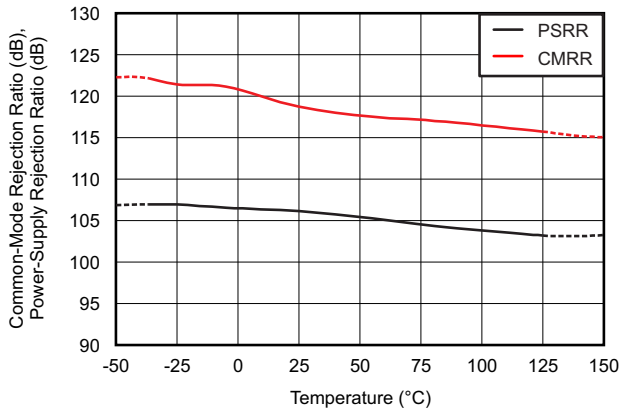


Figure 11. CMRR and PSRR vs Frequency

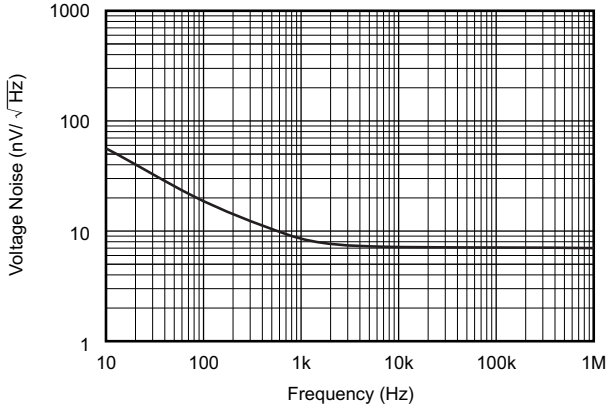


V_S = 1.8 to 5.5 V

Figure 12. CMRR and PSRR vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ, unless otherwise noted.



V_S = 1.8 to 5.5 V

Figure 13. Input Voltage Noise Spectral Density vs Frequency

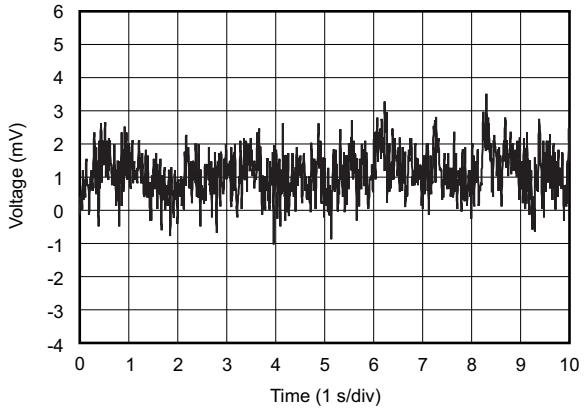
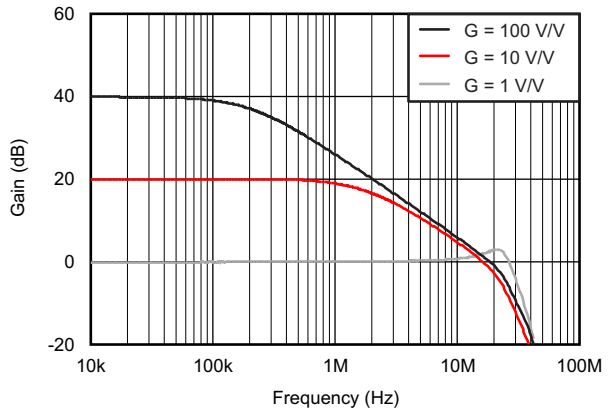
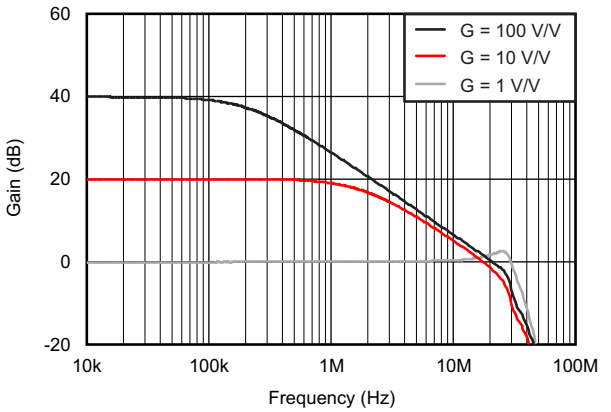


Figure 14. 0.1-Hz to 10-Hz Input Voltage Noise



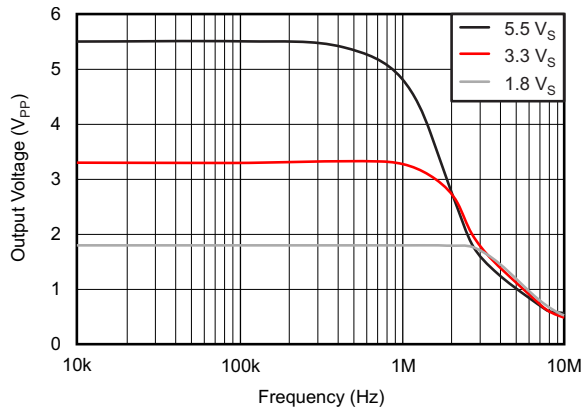
V_S = 1.8 V $C_{(L)}$ = 50 pF $R_{(L)}$ = 10 kΩ

Figure 15. Closed-Loop Gain vs Frequency



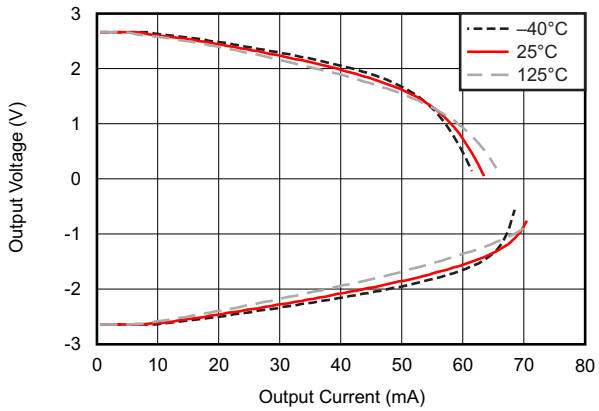
V_S = 5.5 V $C_{(L)}$ = 50 pF $R_{(L)}$ = 10 kΩ

Figure 16. Closed-Loop Gain vs Frequency



$C_{(L)}$ = 50 pF $R_{(L)}$ = 10 kΩ

Figure 17. Maximum Output Voltage vs Frequency

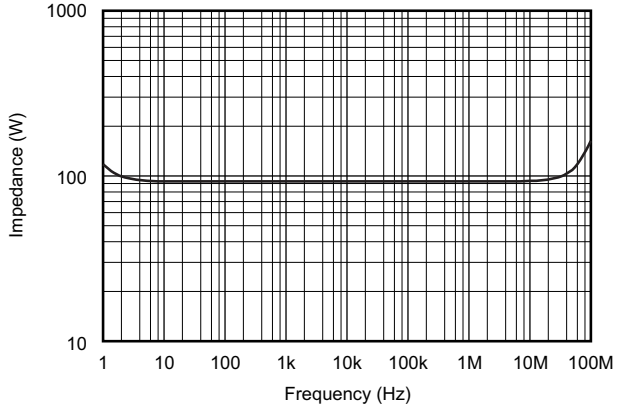


V_S = ±2.75 V

Figure 18. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ, unless otherwise noted.



V_S = ±2.75 V

Figure 19. Open-Loop Output Impedance vs Frequency

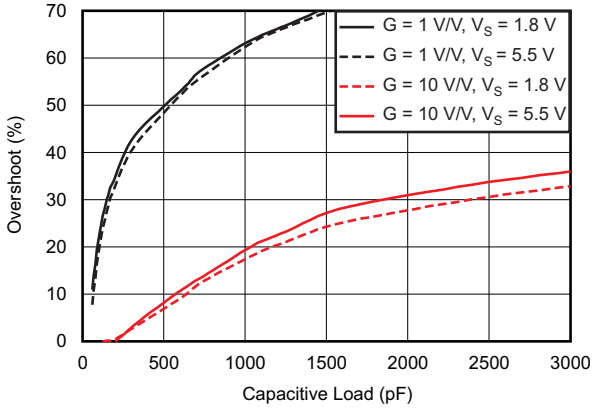
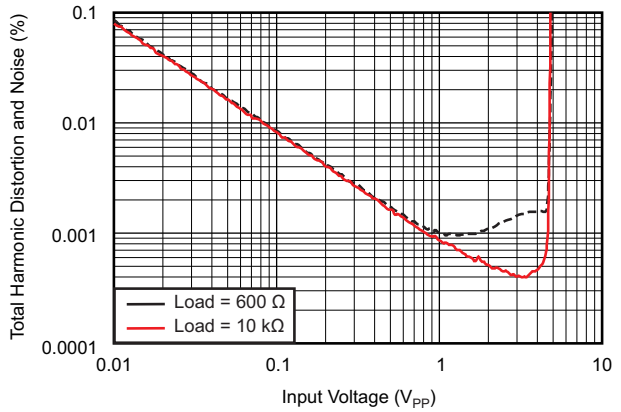
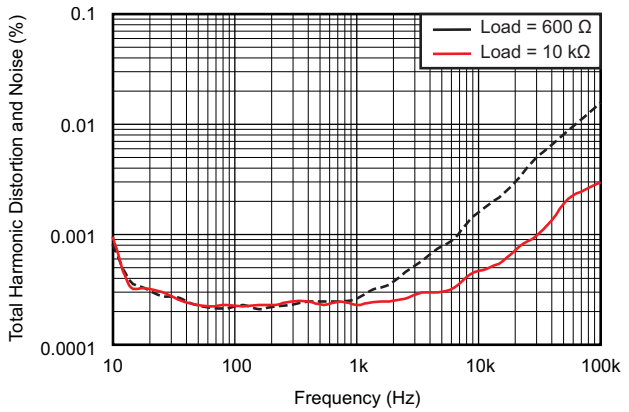


Figure 20. Small-Signal Overshoot vs Load Capacitance



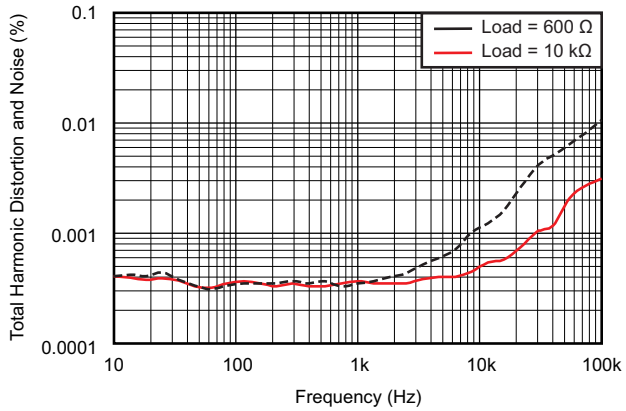
V_S = ±2.5 V f = 10 kHz G = 1 V/V

Figure 21. THD+N vs Amplitude



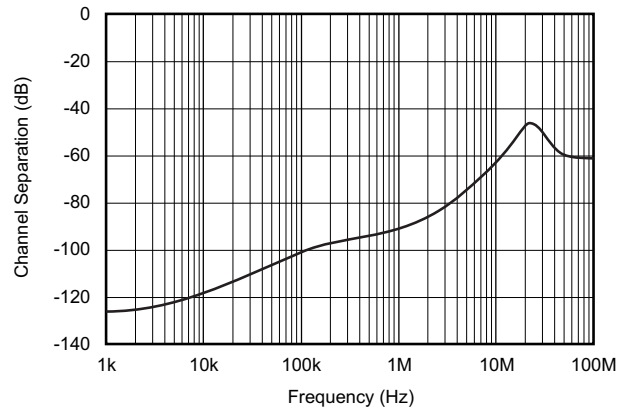
V_S = ±2.5 V f = 10 kHz G = 1 V/V
V_I = 2 V_{PP}

Figure 22. THD+N vs Frequency



V_S = ±2.5 V f = 10 kHz G = 1 V/V
V_I = 4 V_{PP}

Figure 23. THD+N vs Frequency

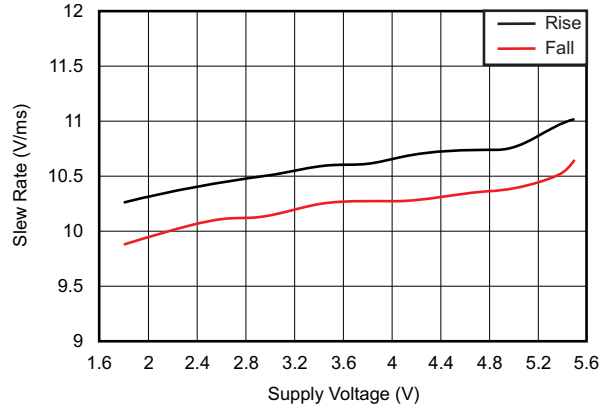


V_S = ±2.75 V

Figure 24. Channel Separation vs Frequency

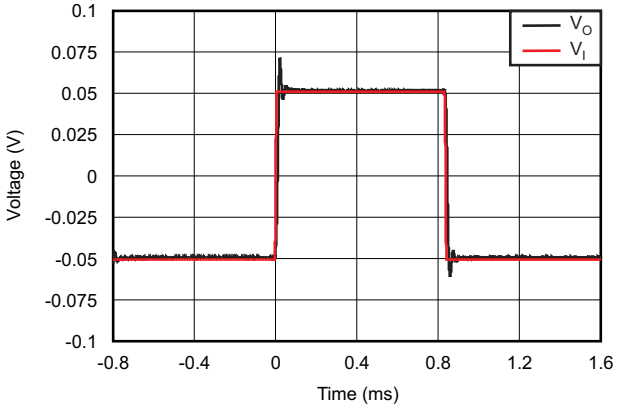
Typical Characteristics (continued)

At T_A = 25°C, $V_{(CM)}$ = V_O = mid-supply, and $R_{(L)}$ = 10 kΩ, unless otherwise noted.



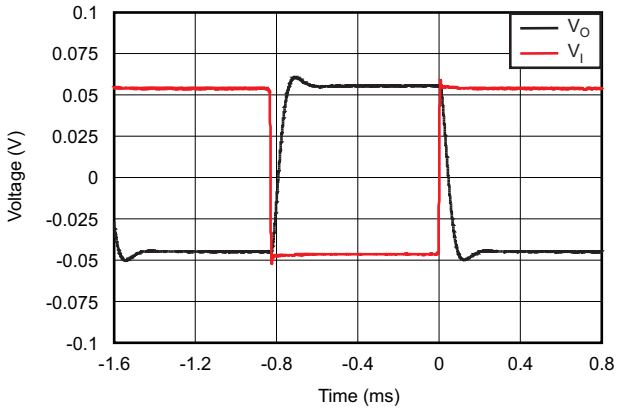
$C_{(L)}$ = 50 pF

Figure 25. Slew Rate vs Supply Voltage



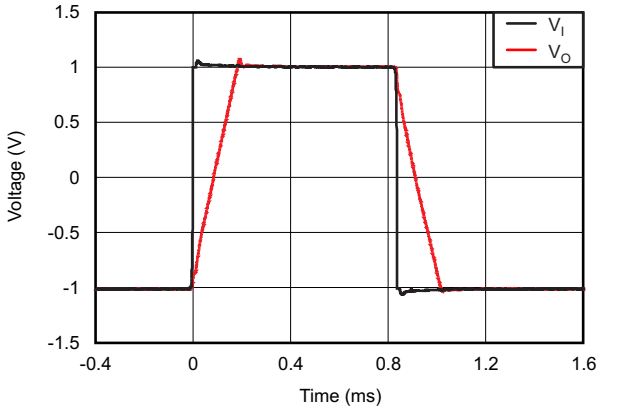
V_S = ±2.75 V G = 1 V/V V_I = 100 mV_{PP}

Figure 26. Small-Signal Step Response



V_S = ±2.75 V G = –1 V/V V_I = 100 mV_{PP}

Figure 27. Small-Signal Step Response



V_S = ±2.75 V G = 1 V/V V_I = 2 V_{PP}

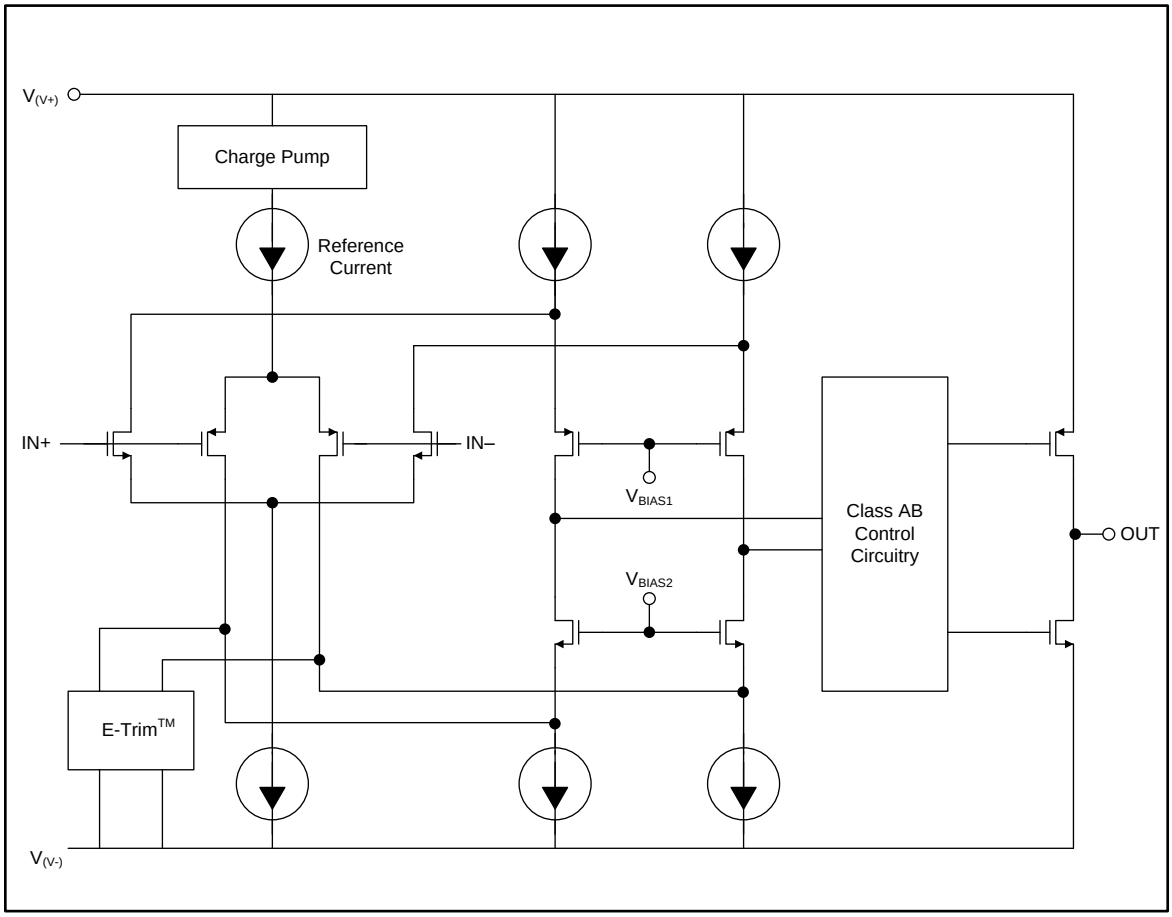
Figure 28. Large-Signal Step Response vs Time

7 Detailed Description

7.1 Overview

The OPA2320-Q1 operational amplifier (op amp) is unity-gain stable and can operate on a single-supply voltage (1.8 V to 5.5 V), or a split supply voltage (±0.9 V to ±2.75 V), making it highly versatile and easy to use. The OPA2320-Q1 device amplifier is fully specified from 1.8 V to 5.5 V and over the extended temperature range of –40°C to 125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Input and ESD Protection

The OPA2320-Q1 device incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, provided that the current is limited to 10 mA as stated in the *Absolute Maximum Ratings* . Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 29 shows how a series input resistor ($R_{(S)}$) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

Feature Description (continued)

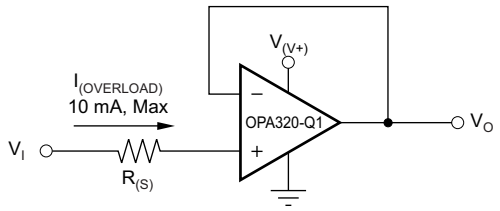
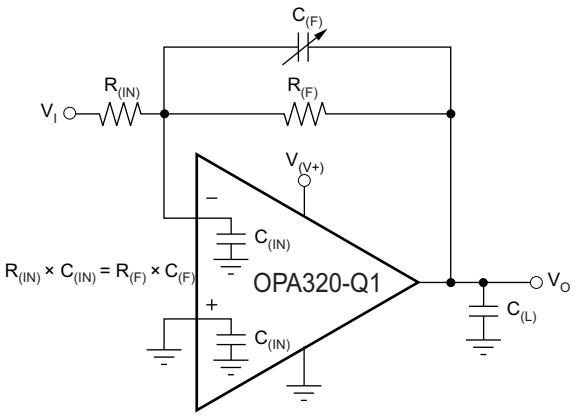


Figure 29. Input Current Protection

7.3.2 Fefeedback Capacitor Improves Response

For optimum settling time and stability with high-impedance feedback networks, adding a feedback capacitor across the feedback resistor, $R_{(FB)}$, as shown in Figure 30 may be necessary. This capacitor compensates for the zero created by the feedback network impedance and the OPA2320-Q1 device input capacitance (and any parasitic layout capacitance). The effect becomes more significant with higher impedance networks.



Note: Where $C_{(IN)}$ is equal to the OPA2320-Q1 input capacitance (approximately 9 pF) plus any parasitic layout capacitance.

Figure 30. Feedback Capacitor Improves Dynamic Performance

It is suggested that a variable capacitor be used for the feedback capacitor because input capacitance may vary between op amps and layout capacitance is difficult to determine. For the circuit shown in Figure 30, the value of the variable feedback capacitor should be chosen so that the input resistance times the input capacitance of the OPA2320-Q1 device (9 pF typical) plus the estimated parasitic layout capacitance equals the feedback capacitor times the feedback resistor:

$$R_{(IN)} \times C_{(IN)} = R_{(FB)} \times C_{(FB)} \quad (1)$$

Where:

- $C_{(IN)}$ is equal to the OPA2320-Q1 input capacitance (sum of differential and common-mode) plus the layout capacitance.

The capacitor value can be adjusted until optimum performance is obtained.

7.3.3 EMI Susceptibility And Input Filtering

Operational amplifiers vary in susceptibility to electromagnetic interference (EMI). If conducted EMI enters the operational amplifier, the DC offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all operational amplifier pin functions can be affected by EMI, the input pins are likely to be the most susceptible. The OPA2320-Q1 operational amplifier family incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by the input filter. The filter is designed for a cut-off frequency of approximately 580 MHz (–3 dB), with a roll-off of 20 dB per decade.

Feature Description (continued)

7.3.4 Output Impedance

The open-loop output impedance of the OPA2320-Q1 common-source output stage is approximately 90 Ω. When the op amp is connected with feedback, this value is reduced significantly by the loop gain. For example, with 130 dB (typical) of open-loop gain, the output impedance is reduced in unity-gain to less than 0.03 Ω. For each decade rise in the closed-loop gain, the loop gain is reduced by the same amount, which results in a ten-fold increase in effective output impedance. While the OPA2320-Q1 output impedance remains very flat over a wide frequency range, at higher frequencies the output impedance rises as the open-loop gain of the op amp drops. However, at these frequencies the output also becomes capacitive as a result of parasitic capacitance. This in turn prevents the output impedance from becoming too high, which can cause stability problems when driving large capacitive loads. As mentioned previously, the OPA2320-Q1 device has excellent capacitive load drive capability for an op amp with the bandwidth.

7.3.5 Capacitive Load and Stability

The OPA2320-Q1 device is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA2320-Q1 device can become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier is stable in operation. An op amp in the unity-gain (1 V/V) buffer configuration and driving a capacitive load exhibits a greater tendency to become unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA2320-Q1 device remains stable with a pure capacitive load up to approximately 1 nF.

The equivalent series resistance (ESR) of some very large capacitors ($C_{(L)}$ > 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains, as shown in Figure 32. One technique for increasing the capacitive load drive capability of the amplifier operating in unity gain is to insert a small resistor ($R_{(S)}$), typically 10 Ω to 20 Ω, in series with the output, as shown in Figure 31.

This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. A possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing. The error contributed by the voltage divider may be insignificant. For instance, with a load resistance, $R_{(L)}$ = 10 kΩ and $R_{(S)}$ = 20 Ω, the gain error is only about 0.2%. However, when $R_{(L)}$ is decreased to 600 Ω, which the OPA2320-Q1 device is able to drive, the error increases to 7.5%.

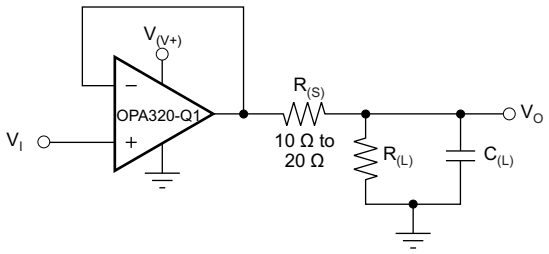


Figure 31. Improving Capacitive Load Drive

Feature Description (continued)

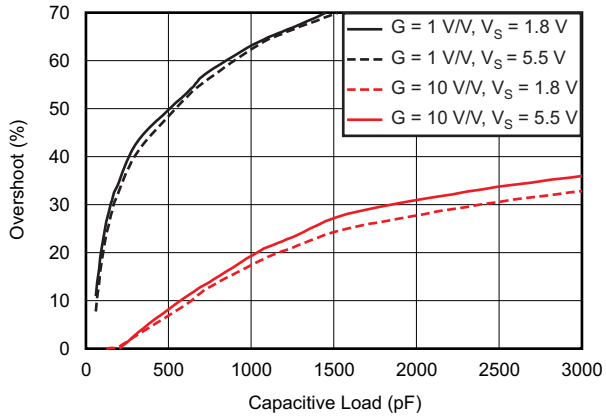


Figure 32. Small-Signal Overshoot versus Capacitive Load (100-mV$_{PP}$ Output Step)

7.3.6 Overload Recovery Time

Overload recovery time is the time it takes the output of the amplifier to come out of saturation and recover to the linear region. Overload recovery is particularly important in applications where small signals must be amplified in the presence of large transients. Figure 33 and Figure 34 show the positive and negative overload recovery times of the OPA2320-Q1 device, respectively. In both cases, the time elapsed before the OPA2320-Q1 device comes out of saturation is less than 100 ns. In addition, the symmetry between the positive and negative recovery times allows excellent signal rectification without distortion of the output signal.

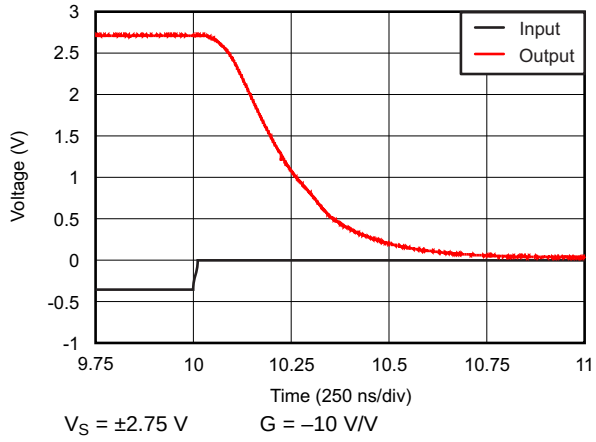


Figure 33. Positive Recovery Time

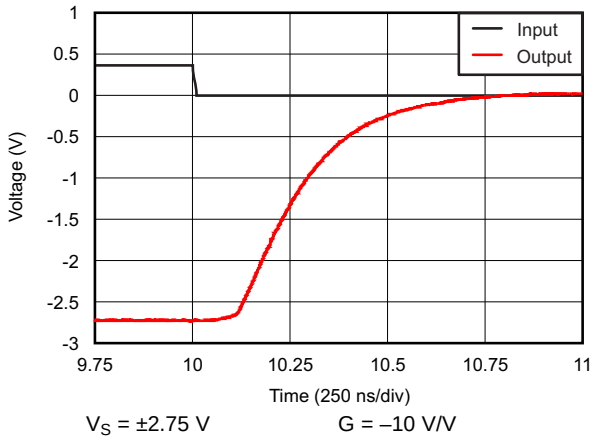


Figure 34. Negative Recovery Time

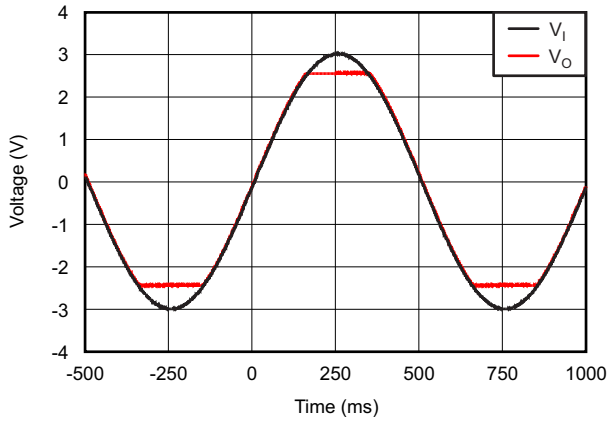
7.4 Device Functional Modes

7.4.1 Rail-to-Rail Input

The OPA2320-Q1 device features true rail-to-rail input operation, with supply voltages as low as ±0.9 V (1.8 V). The design of the OPA2320-Q1 amplifiers include an internal charge-pump that powers the amplifier input stage with an internal supply rail at approximately 1.6 V above the external supply (V+). This internal supply rail allows the single differential input pair to operate and remain very linear over a very wide input common-mode range. A unique zero-crossover input topology eliminates the input offset transition region typical of many rail-to-rail, complementary input stage operational amplifiers. This topology allows the OPA2320-Q1 device to provide superior common-mode performance (CMRR > 110 dB, typical) over the entire common-mode input range, which extends 100 mV beyond both power-supply rails. When driving analog-to-digital converters (ADCs), the highly linear $V_{(CM)}$ range of the OPA2320-Q1 device assures maximum linearity and lowest distortion.

7.4.2 Phase Reversal

The OPA2320-Q1 op amp is designed to be immune to phase reversal when the input pins exceed the supply voltages, therefore providing further in-system stability and predictability. Figure 35 shows the input voltage exceeding the supply voltage without any phase reversal.



V_S = ±2.5 V

Figure 35. No Phase Reversal

8 Application And Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

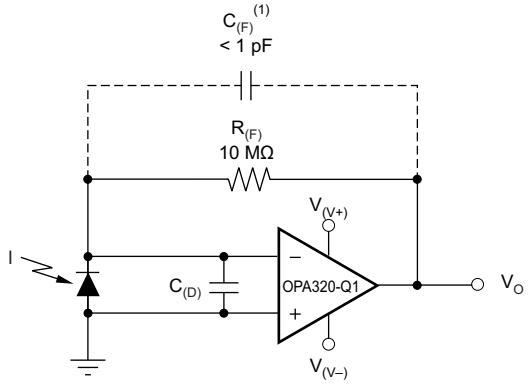
The OPA2320-Q1 device can be used in a wide range of applications such as a transimpedance amplifier, high-impedance sensor, active filter, and for driving ADCs.

8.2 Typical Applications

8.2.1 Transimpedance Amplifier

Wide gain bandwidth, low input bias current, low input voltage, and current noise make the OPA2320-Q1 device an ideal wideband photodiode transimpedance amplifier. Low-voltage noise is important because photodiode capacitance causes the effective noise gain of the circuit to increase at high frequency.

The key elements to a transimpedance design, as shown in Figure 36, are the expected diode capacitance ($C_{(D)}$), which should include the parasitic input common-mode and differential-mode input capacitance (4 pF + 5 pF); the desired transimpedance gain ($R_{(FB)}$); and the gain-bandwidth (GBW) for the OPA2320-Q1 device (20 MHz). With these three variables set, the feedback capacitor value ($C_{(FB)}$) can be set to control the frequency response. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$, which is 0.2 pF for a typical surface-mount resistor.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

Figure 36. Dual-Supply Transimpedance Amplifier

8.2.1.1 Design Requirements

PARAMETER	VALUE
Supply voltage $V_{(V+)}$	2.5 V
Supply voltage $V_{(V-)}$	–2.5 V

8.2.1.2 Detailed Design Procedure

To achieve a maximally-flat, second-order Butterworth frequency response, the feedback pole should be set to:

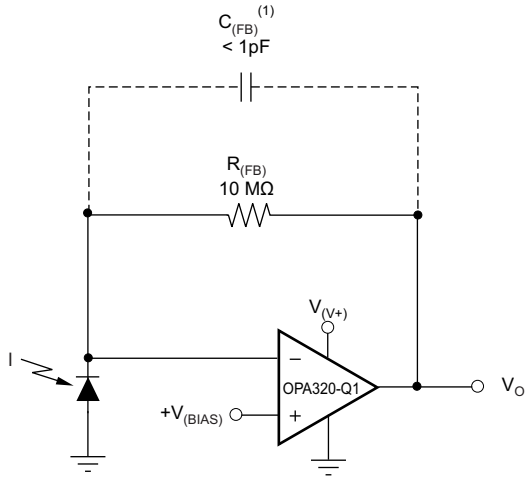
$$\frac{1}{2 \times \pi \times R_{(FB)} \times C_{(FB)}} = \sqrt{\frac{GBW}{4 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (2)$$

Use Equation 3 to calculate the bandwidth.

$$f_{(-3\ dB)} = \sqrt{\frac{GBW}{2 \times \pi \times R_{(FB)} \times C_{(D)}}} \quad (3)$$

For even higher transimpedance bandwidth, consider the high-speed CMOS OPA380 (90-MHz GBW), OPA354 (100-MHz GBW), OPA300 (180-MHz GBW), OPA355 (200-MHz GBW), or OPA656 and OPA657 (400-MHz GBW).

For single-supply applications, the +INx input can be biased with a positive DC voltage to allow the output to reach true zero when the photodiode is not exposed to any light, and respond without the added delay that results from coming out of the negative rail; this configuration is shown in Figure 37. This bias voltage also appears across the photodiode, providing a reverse bias for faster operation.



(1) $C_{(FB)}$ is optional to prevent gain peaking. $C_{(FB)}$ includes the stray capacitance of $R_{(FB)}$.

Figure 37. Single-Supply Transimpedance Amplifier

For additional information, refer to the application bulletin from TI, *Compensate Transimpedance Amplifiers Intuitively* (SBOA055).

8.2.1.2.1 Optimizing The Transimpedance Circuit

To achieve the best performance, components should be selected according to the following guidelines:

1. For lowest noise, select $R_{(FB)}$ to create the total required gain. Using a lower value for $R_{(FB)}$ and adding gain after the transimpedance amplifier generally produces poorer noise performance. The noise produced by $R_{(FB)}$ increases with the square-root of $R_{(FB)}$, whereas the signal increases linearly. Therefore, signal-to-noise ratio improves when all the required gain is placed in the transimpedance stage.
2. Minimize photodiode capacitance and stray capacitance at the summing junction (inverting input). This capacitance causes the voltage noise of the op amp to be amplified (increasing amplification at high frequency). Using a low-noise voltage source to reverse-bias a photodiode can significantly reduce the capacitance. Smaller photodiodes have lower capacitance. Use optics to concentrate light on a small photodiode.
3. Noise increases with increased bandwidth. Limit the circuit bandwidth to only that required. Use a capacitor across the $R_{(FB)}$ to limit bandwidth, even if not required for stability.
4. Circuit board leakage can degrade the performance of an otherwise well-designed amplifier. Clean the circuit board carefully. A circuit board guard trace that encircles the summing junction and is driven at the same voltage can help control leakage.

For additional information, refer to the following application bulletins from TI: *Noise Analysis of FET Transimpedance Amplifiers* (SBOA060), and *Noise Analysis for High-Speed Op Amps* (SBOA066).

8.2.1.3 Application Curves

Wide gain bandwidth as shown in Figure 38 and low input voltage noise as shown in Figure 39 make the OPA2320-Q1 device an ideal wideband photodiode transimpedance amplifier.

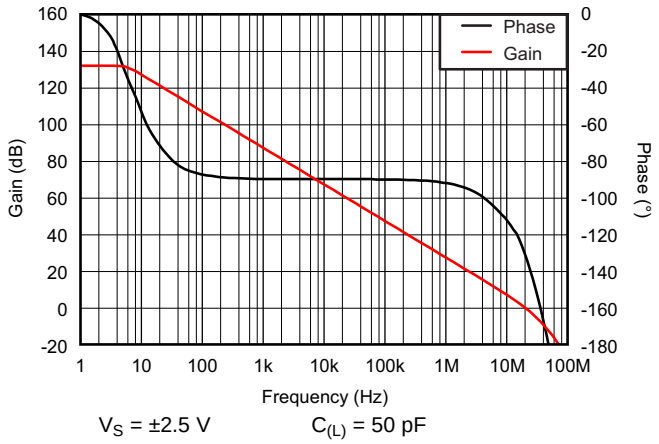


Figure 38. Open-Loop Gain and Phase vs Frequency

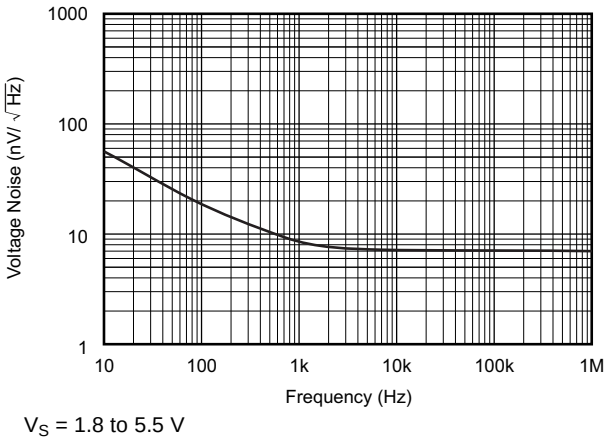


Figure 39. Input Voltage Noise Spectral Density vs Frequency

8.2.2 High-Impedance Sensor Interface

Many sensors have high source impedances that may range up to 10 MΩ, or even higher. The output signal of sensors often must be amplified or otherwise conditioned by means of an amplifier. The input bias current of this amplifier can load the sensor output and cause a voltage drop across the source resistance, as shown in Figure 40, where ($V_{(+INx)} = V_S - I_{(BIAS)} \times R_{(S)}$). The last term, $I_{(BIAS)} \times R_{(S)}$, shows the voltage drop across $R_{(S)}$. To prevent errors introduced to the system as a result of this voltage, an op amp with very low input bias current must be used with high impedance sensors. This low current keeps the error contribution by $I_{(BIAS)} \times R_{(S)}$ less than the input voltage noise of the amplifier, so that it does not become the dominant noise factor. The OPA2320-Q1 device series of op amps feature very low input bias current (typically 200 fA), and are therefore ideal choices for such applications.

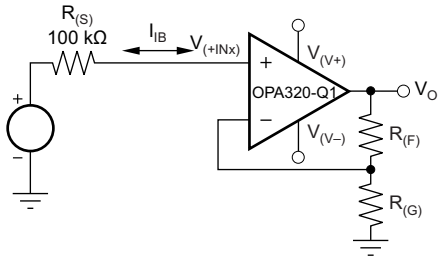


Figure 40. Noise as a Result of $I_{(BIAS)}$

8.2.3 Driving ADCs

The OPA2320-Q1 device series op amps are well-suited for driving sampling analog-to-digital converters (ADCs) with sampling speeds up to 1 MSPS. The zero-crossover distortion input stage topology allows the OPA2320-Q1 device to drive ADCs without degradation of differential linearity and THD.

The OPA2320-Q1 device can be used to buffer the ADC switched input capacitance and resulting charge injection while providing signal gain. Figure 42 shows the OPA2320-Q1 device configured to drive the ADS8326.

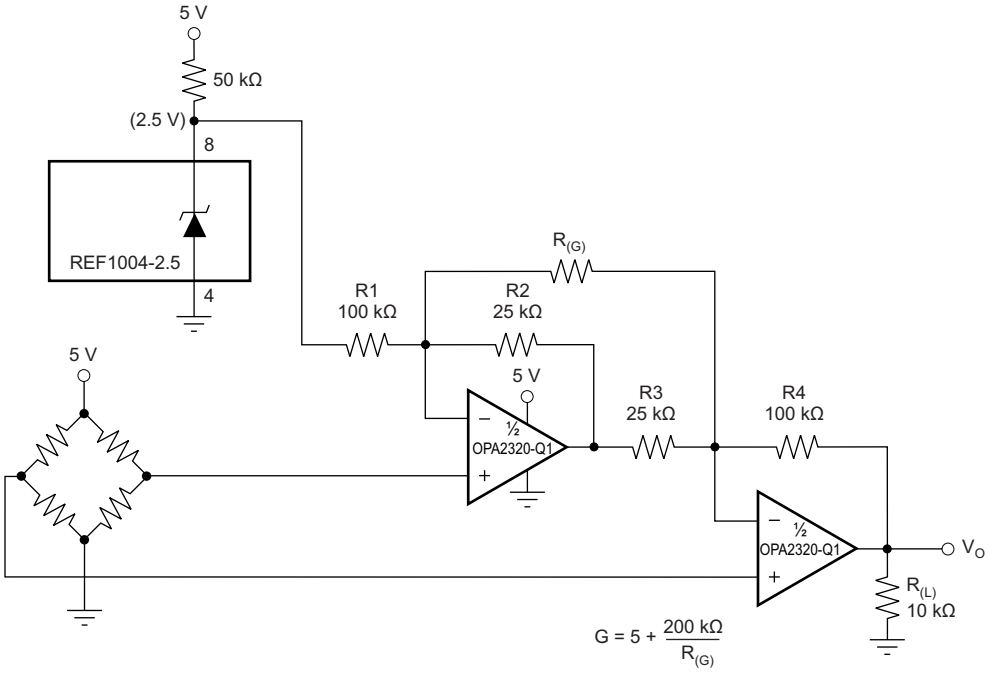
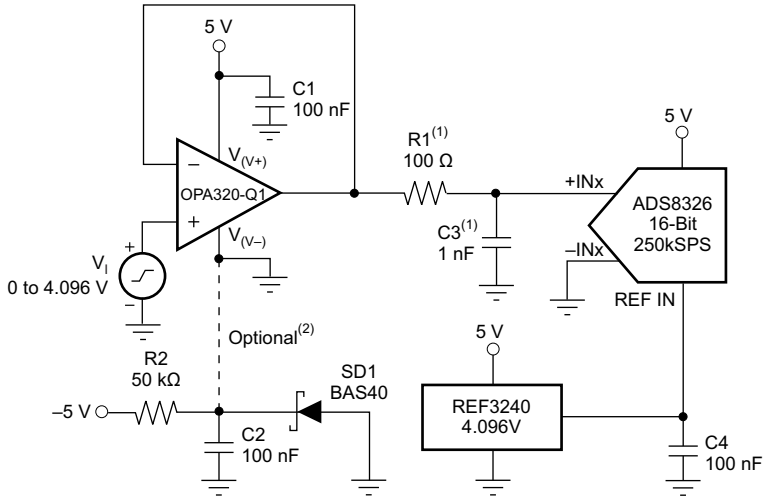


Figure 41. Two Op-Amp Instrumentation Amplifier With Improved High-Frequency Common-Mode Rejection



(1) Suggested value; may require adjustment based on specific application.

(2) Single-supply applications lose a small number of ADC codes near ground as a result of op amp output swing limitation. If a negative power supply is available, this simple circuit creates a –0.3-V supply to allow output swing to true ground potential.

Figure 42. Driving the ADS8326

8.2.4 Active Filter

The OPA2320-Q1 device is well-suited for active filter applications that require a wide bandwidth, fast slew rate, low-noise, single-supply operational amplifier. Figure 43 shows a 500 kHz, second-order, low-pass filter using the multiple-feedback (MFB) topology. The components have been selected to provide a maximally-flat Butterworth response. Beyond the cutoff frequency, roll-off is –40 dB/dec. The Butterworth response is ideal for applications requiring predictable gain characteristics, such as the anti-aliasing filter used in front of an ADC.

One point to observe when considering the MFB filter is that the output is inverted, relative to the input. If this inversion is not required, or not desired, a noninverting output can be achieved through one of the following options:

1. adding an inverting amplifier
2. adding an additional second-order MFB stage
3. using a noninverting filter topology, such as the Sallen-Key (see Figure 44).

MFB and Sallen-Key, low-pass and high-pass filter synthesis is quickly accomplished using TI's FilterPro™ program. This software is available as a free download at www.ti.com.

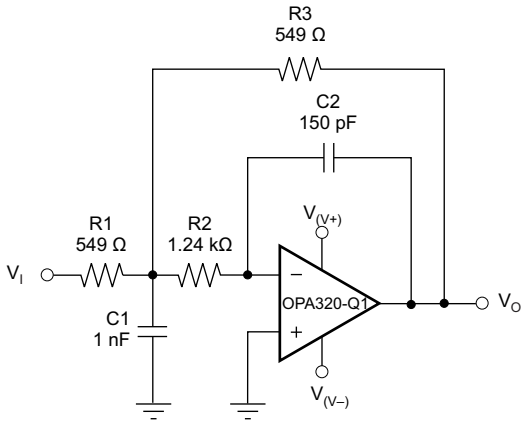


Figure 43. Second-Order Butterworth 500-kHz Low-Pass Filter

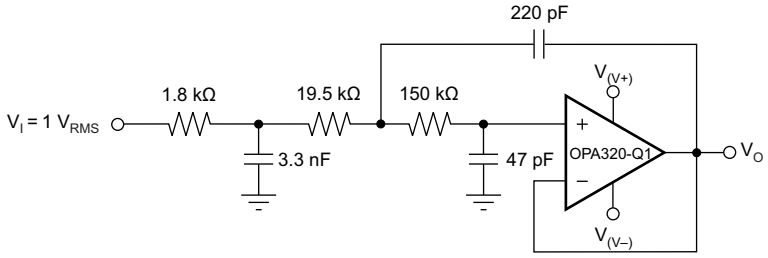


Figure 44. OPA2320-Q1 Configured as a Three-Pole, 20-kHz, Sallen-Key Filter

9 Power Supply Recommendations

The OPA2320-Q1 device is specified for operation from 1.8 to 5.5 V (±0.9 to ±2.75 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics* section.

CAUTION

Supply voltages larger than 6 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

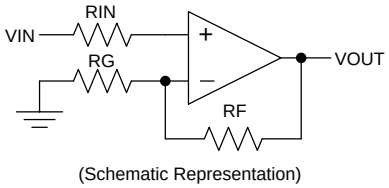
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, refer to *Circuit Board Layout Techniques*, SLOA089.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in , keeping RF and RG close to the inverting input will minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example



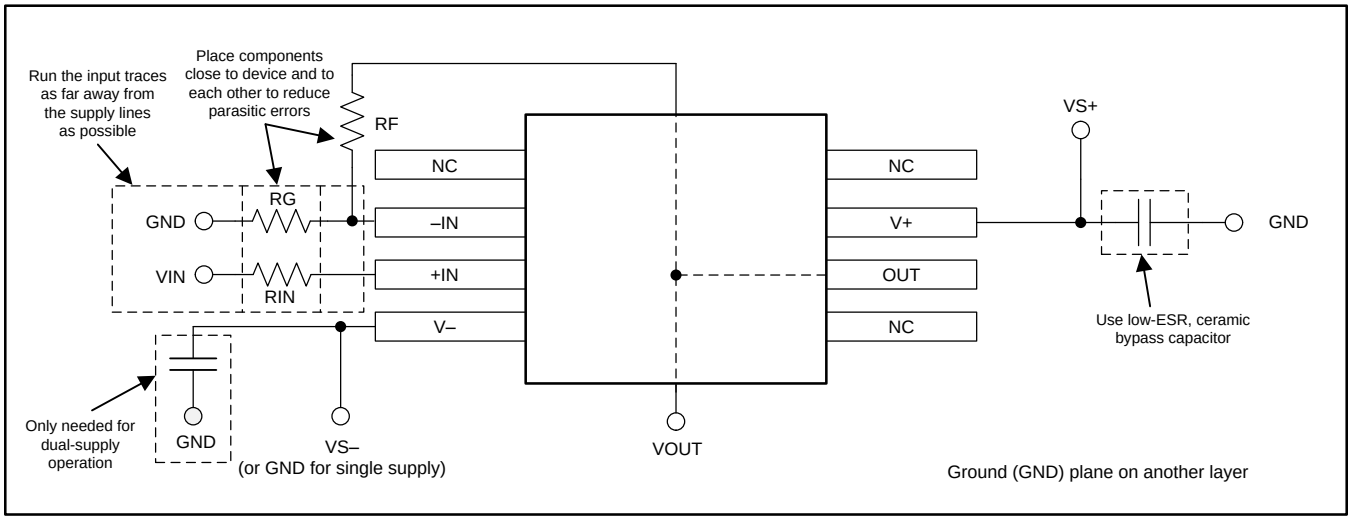


Figure 45. Operational Amplifier Board Layout for Noninverting Configuration

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

For related documentation see the following:

- ADS8326 *16-Bit, High-Speed, 2.7V to 5.5V microPower Sampling ANALOG-TO-DIGITAL CONVERTER*, SBAS343
- *Compensate Transimpedance Amplifiers Intuitively*, SBOA055
- *FilterPro™ User's Guide*, SBFA001
- *NOISE ANALYSIS OF FET TRANSIMPEDANCE AMPLIFIERS*, SBOA060
- *Noise Analysis for High-Speed Op Amps*, SBOA066
- OPA380 and OPA2380 *Precision, High-Speed Transimpedance Amplifier*, SBOS291
- OPA354, OPA2354, and OPA4354 *250MHz, Rail-to-Rail I/O, CMOS OPERATIONAL AMPLIFIERS*, SBOS233
- OPA355, OPA2355, and OPA3355 *200MHz, CMOS OPERATIONAL AMPLIFIER WITH SHUTDOWN*, SBOS195
- OPA656 *Wideband, Unity-Gain Stable, FET-Input OPERATIONAL AMPLIFIER*, SBOS196

11.2 Documentation Support

11.2.1 Related Documentation

11.3 Trademarks

FilterPro is a trademark of Texas Instruments Incorporated.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, And Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2320AQDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	ZAEV	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2320-Q1 :

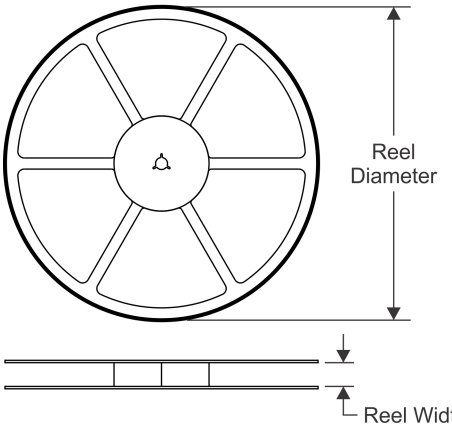
- Catalog: OPA2320

NOTE: Qualified Version Definitions:

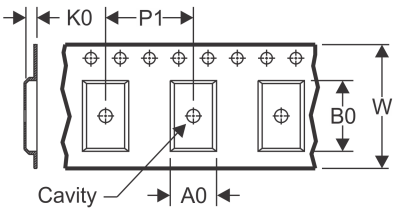
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

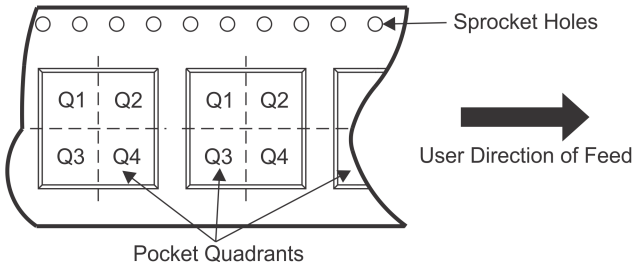


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

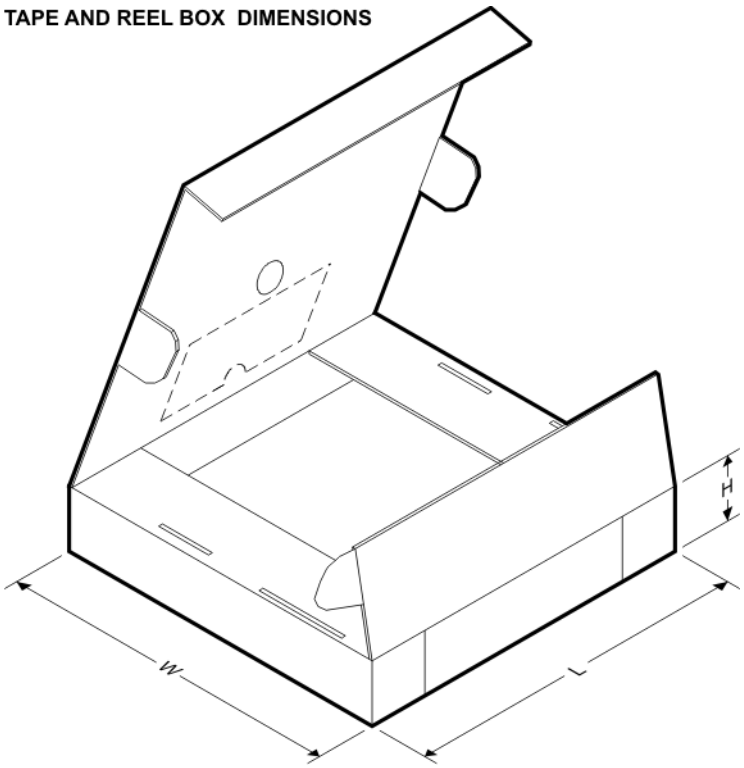
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2320AQDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

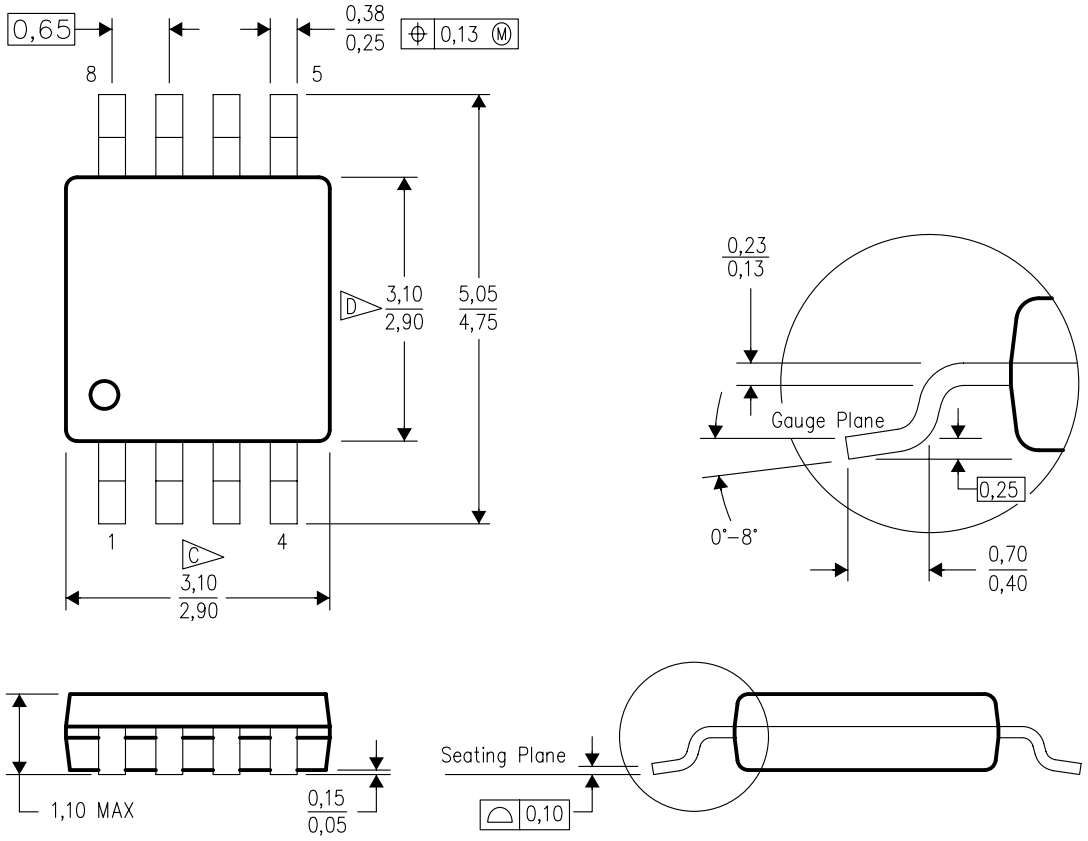
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2320AQDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0

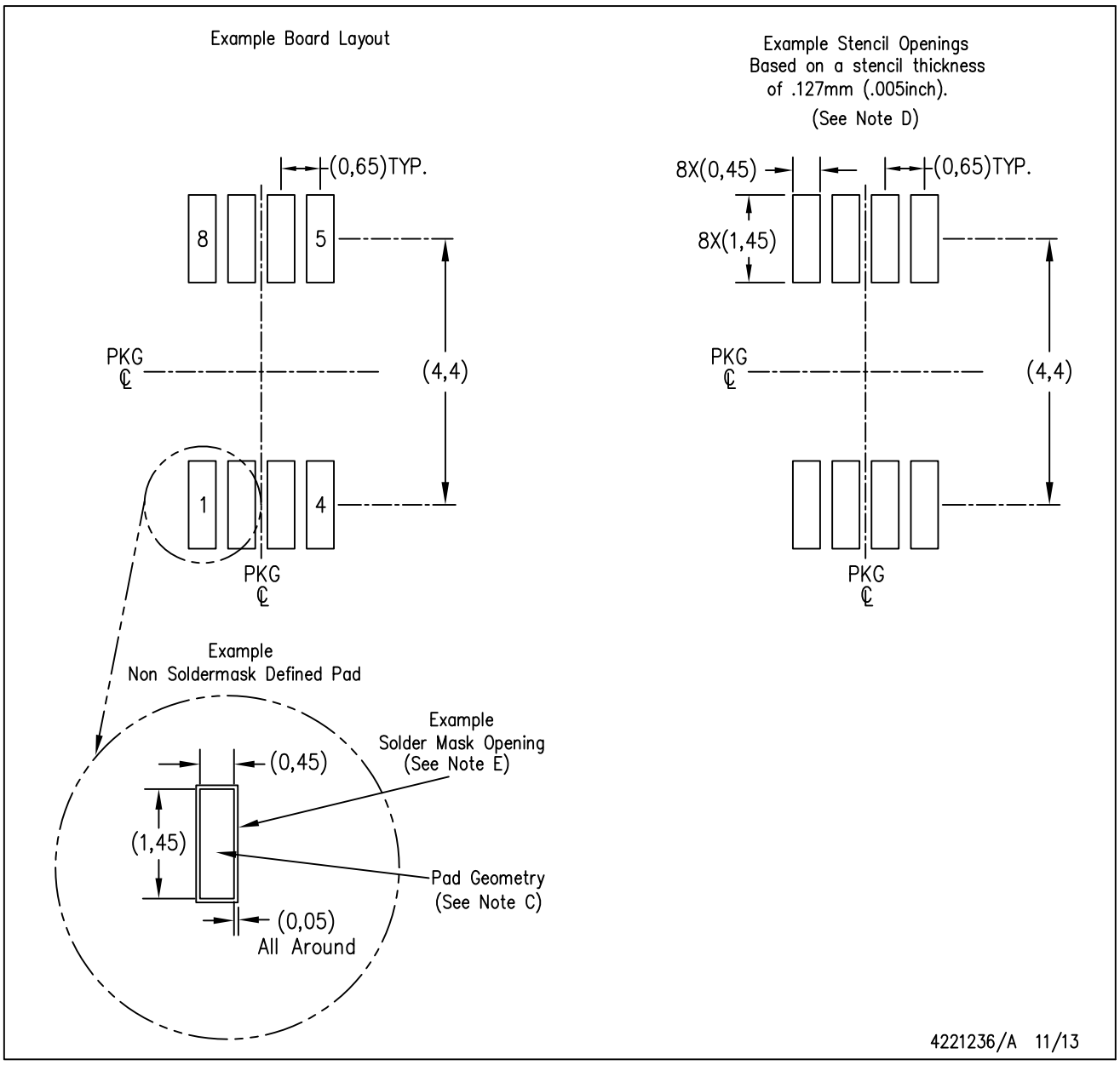
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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