

LCFC Confidential


G Project M/B Schematics Document

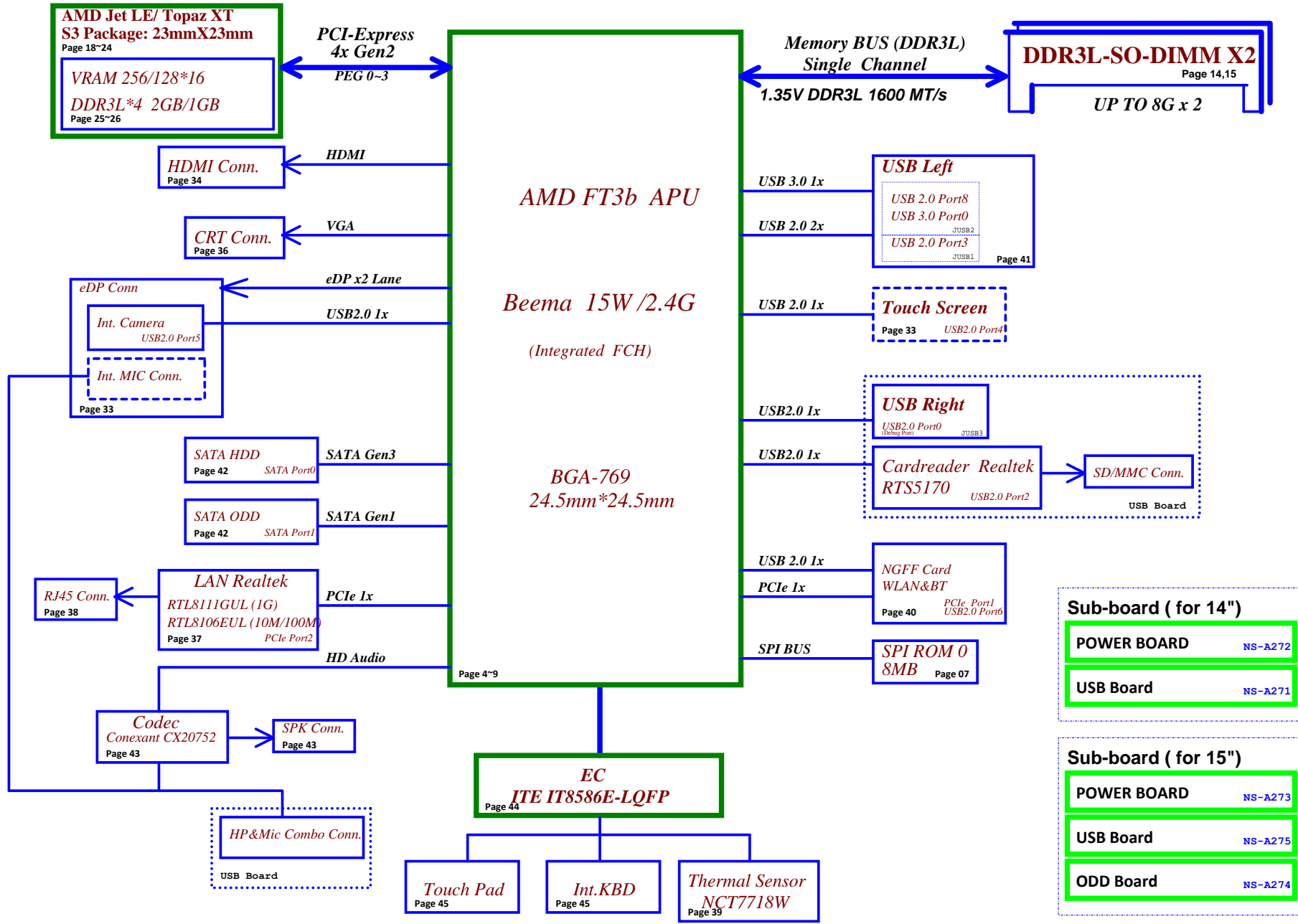
AMD FT3B Beema SOC with DDRIIL

AMD JET-LE

2014-2-12

REV: 0.4

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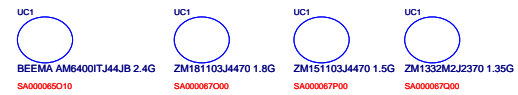
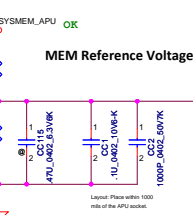
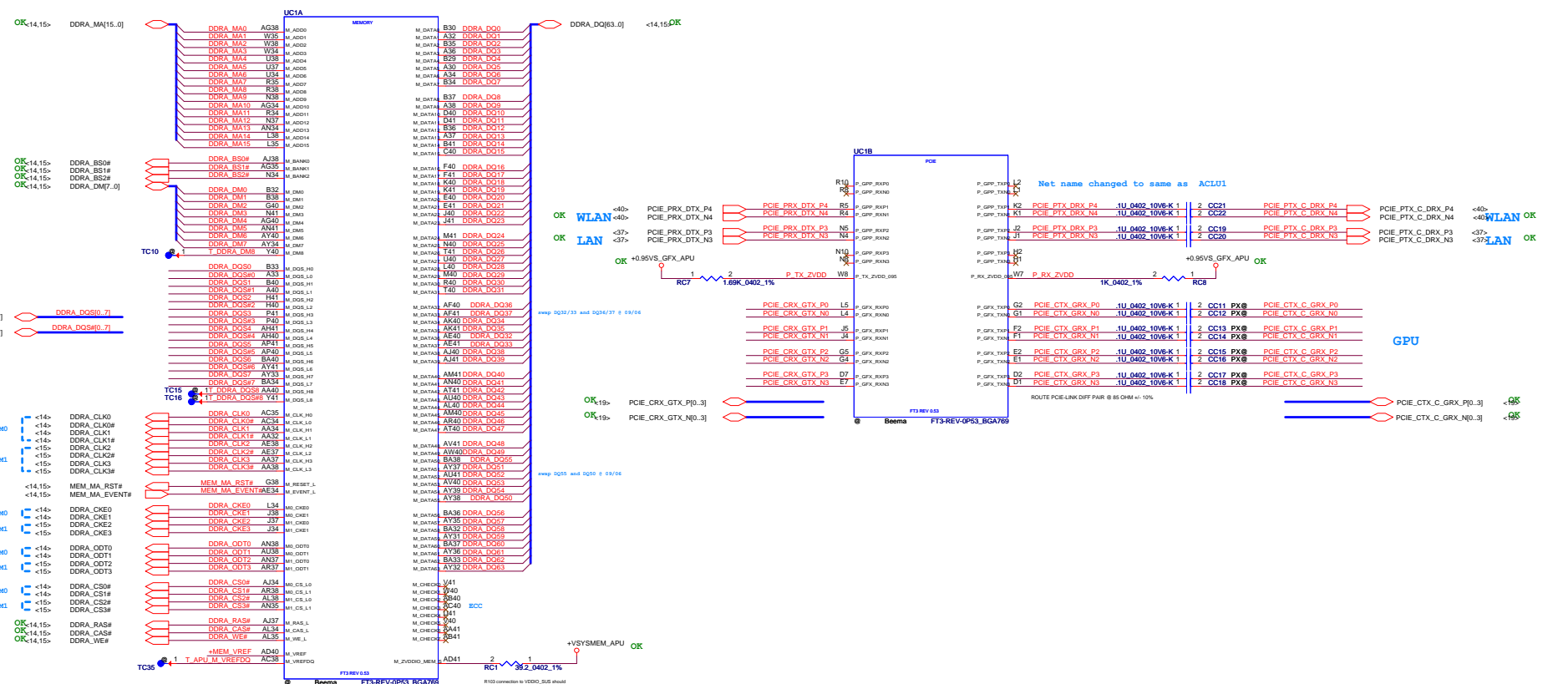
Sub-board (for 14")

- POWER BOARD** NS-A272
- USB Board** NS-A271

Sub-board (for 15")

- POWER BOARD** NS-A273
- USB Board** NS-A275
- ODD Board** NS-A274

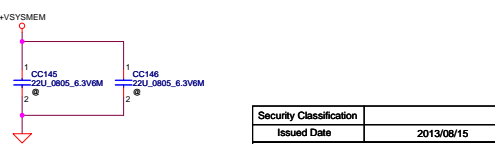
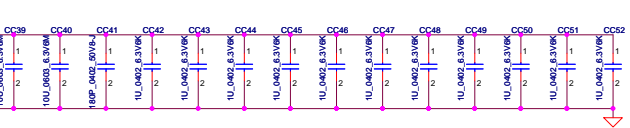
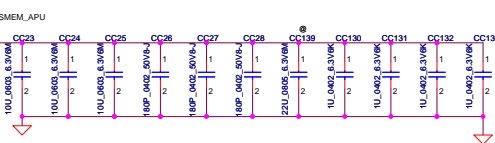
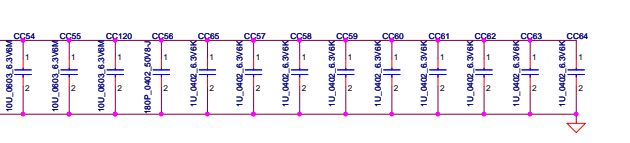
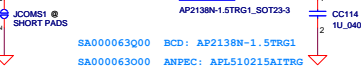
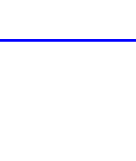
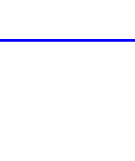
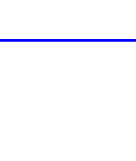
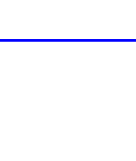
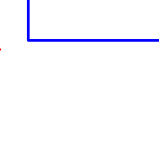
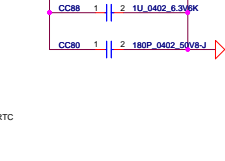
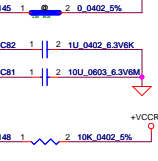
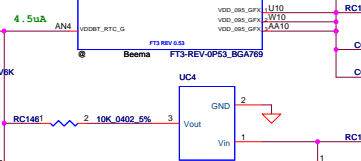
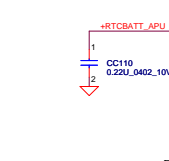
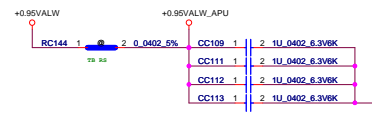
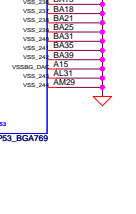
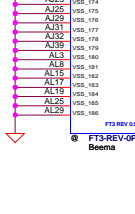
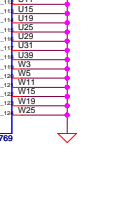
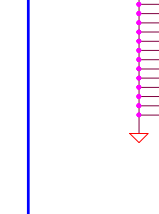
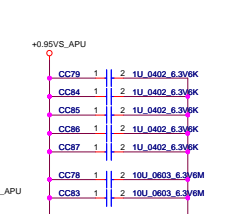
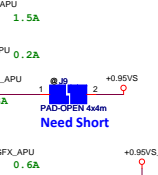
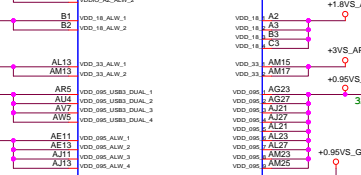
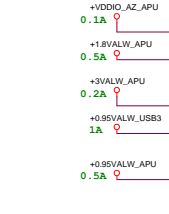
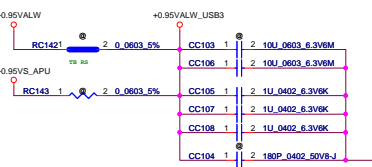
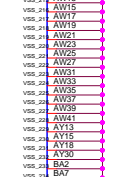
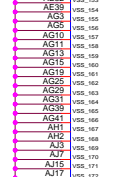
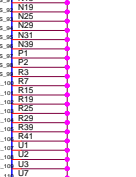
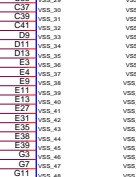
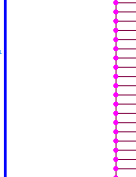
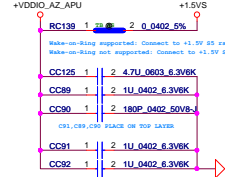
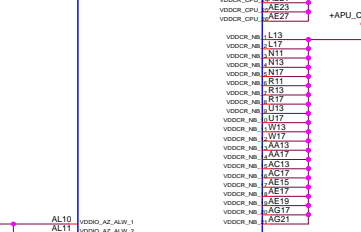
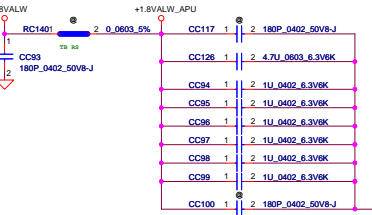
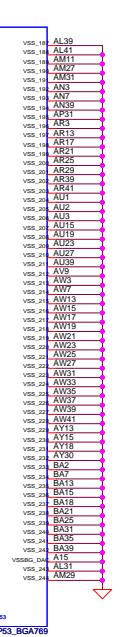
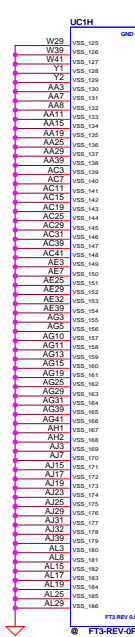
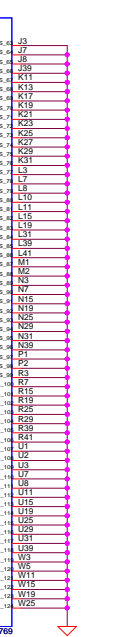
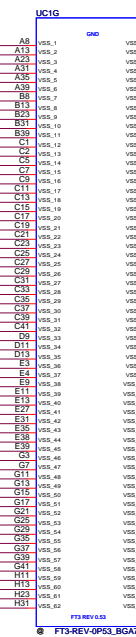
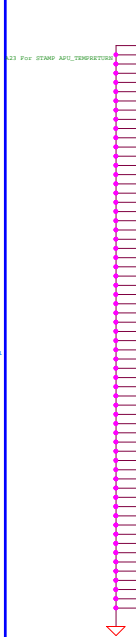
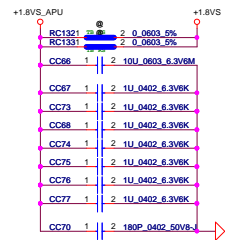
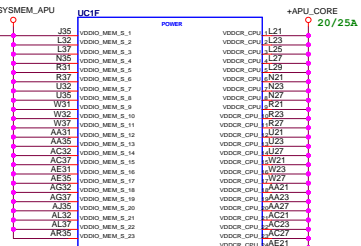
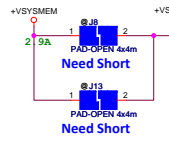
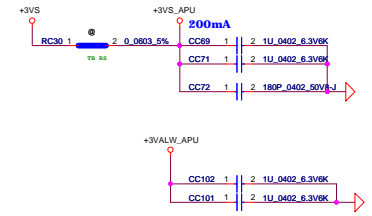
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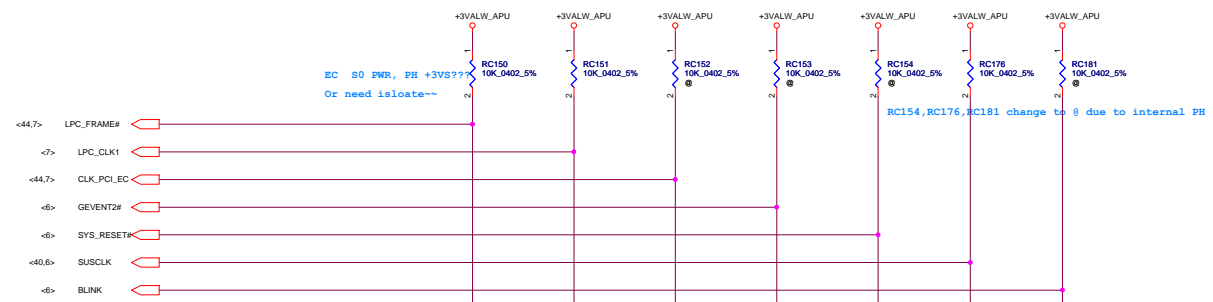


All RLC follow CRB, need double check with DG.



SA000063Q00 BCD: AP2138N-1.5TRG1
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STRAP PINS

Signal	LFRAME_L	LPCCCLK1	LPCCCLK0	GEVENT2_L	SYS_RESET_L	RTCCLK	BLINK
Type	II	II	II	II	I	I	I
PULL HIGH	SPI ROM Default	Internal CLK Gen Default	Boot Fail Timer Enabled	1.8V SPI	Normal Power Up & Reset Timing Default	Coin Battery Default	LDT_RST#/ LDT_PWRGD output to APU Default
PULL LOW	LPC ROM	External CLK Gen	Boot Fail Timer Disabled Default	3.3V SPI Default	Reserved	Direct DC	Reserved

Type I straps become valid immediately after capture with the rising edge of RSMRST_L.
 Type II straps become valid after PWR_GOOD is asserted
 All Strap pins must be configured with either external pull-up or pull-down resistors.

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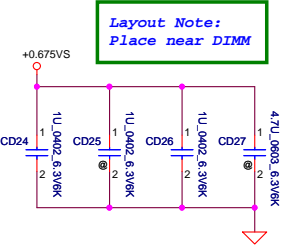
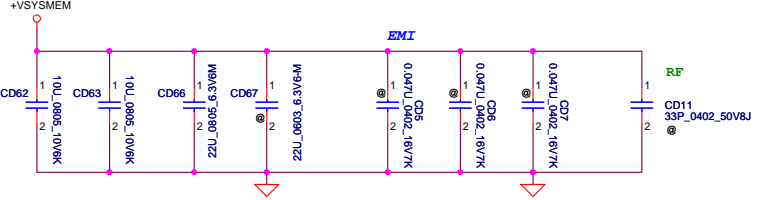
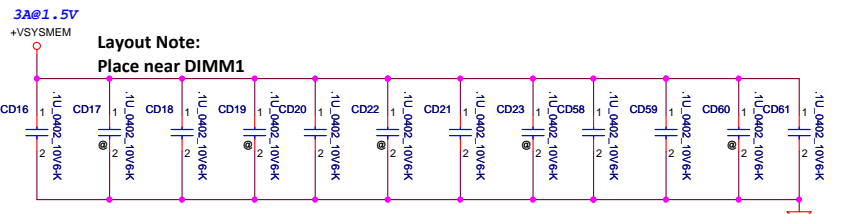
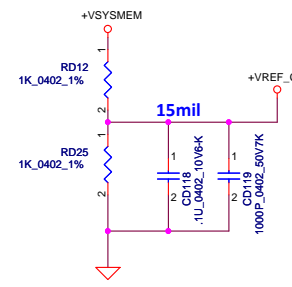
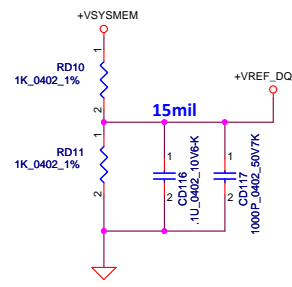
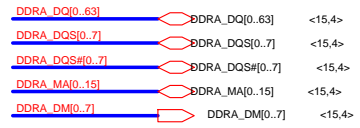
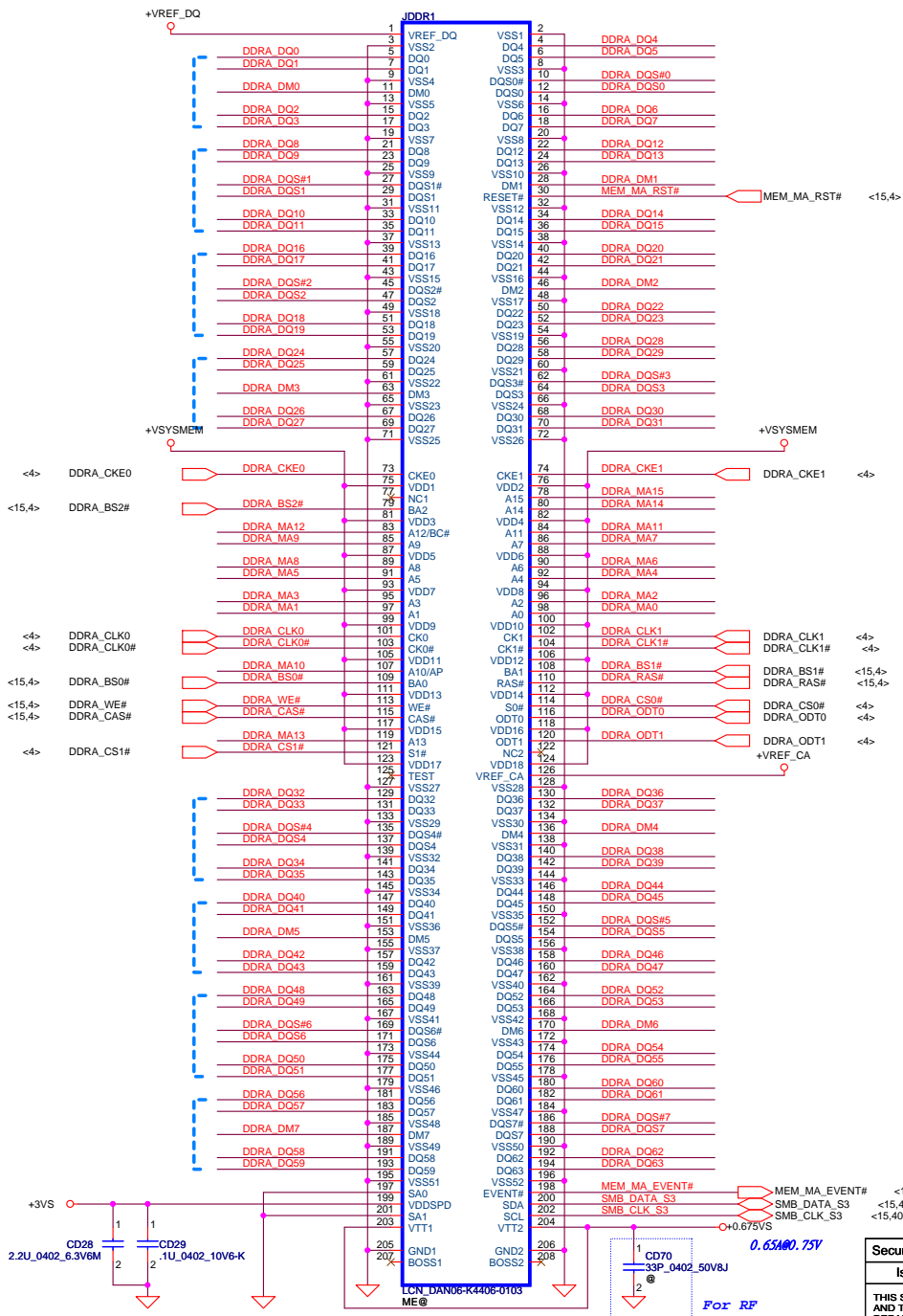
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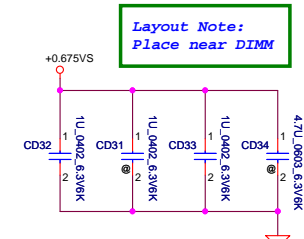
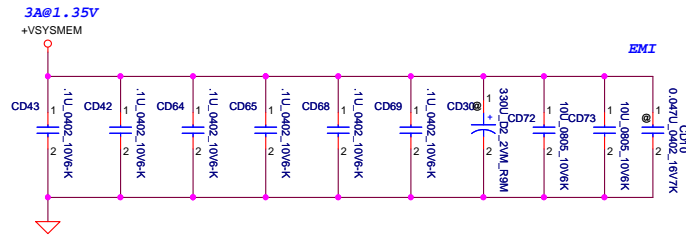
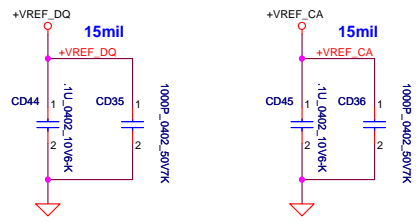
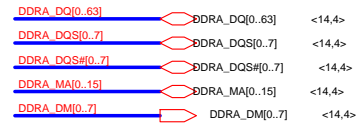
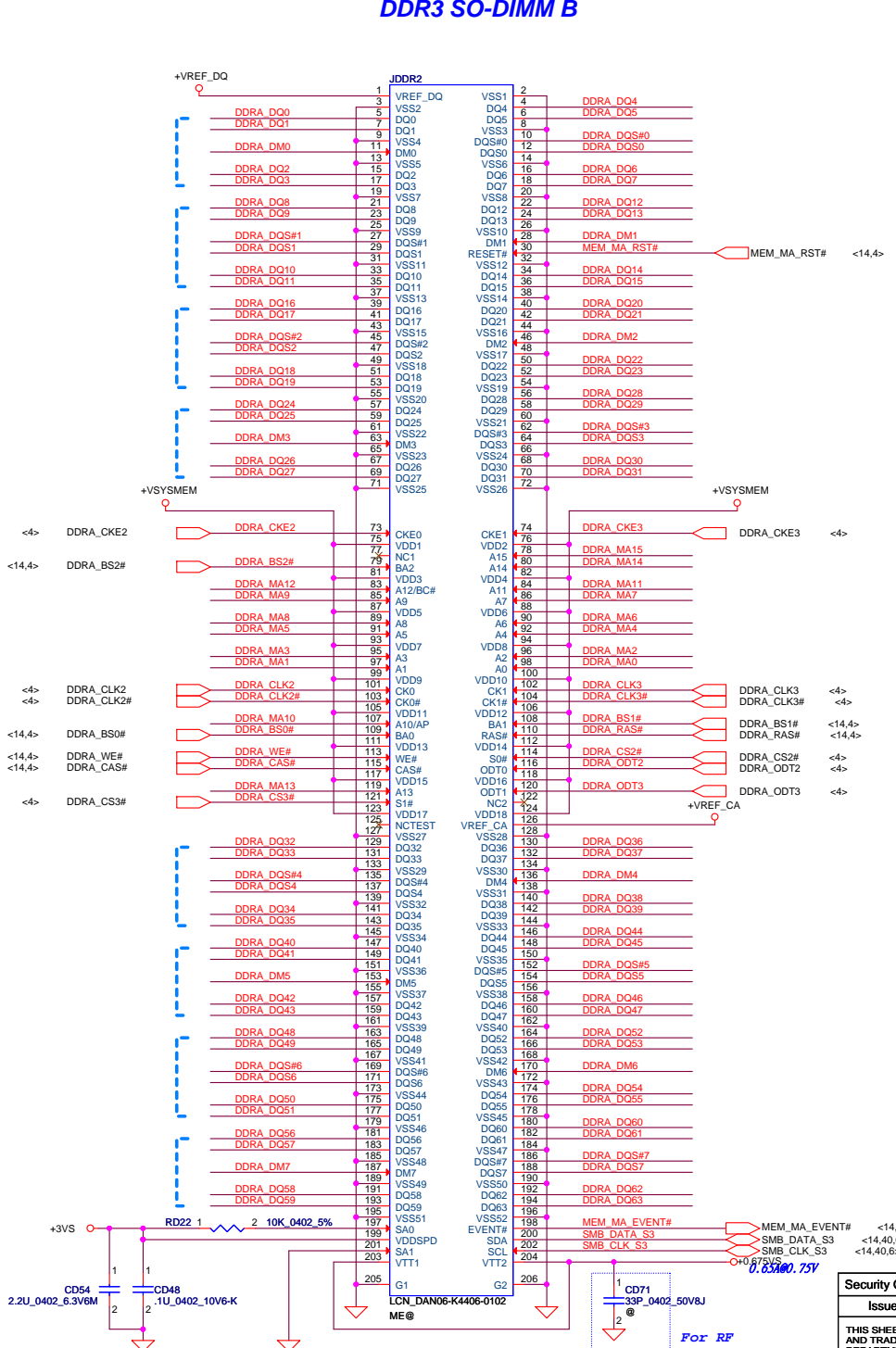
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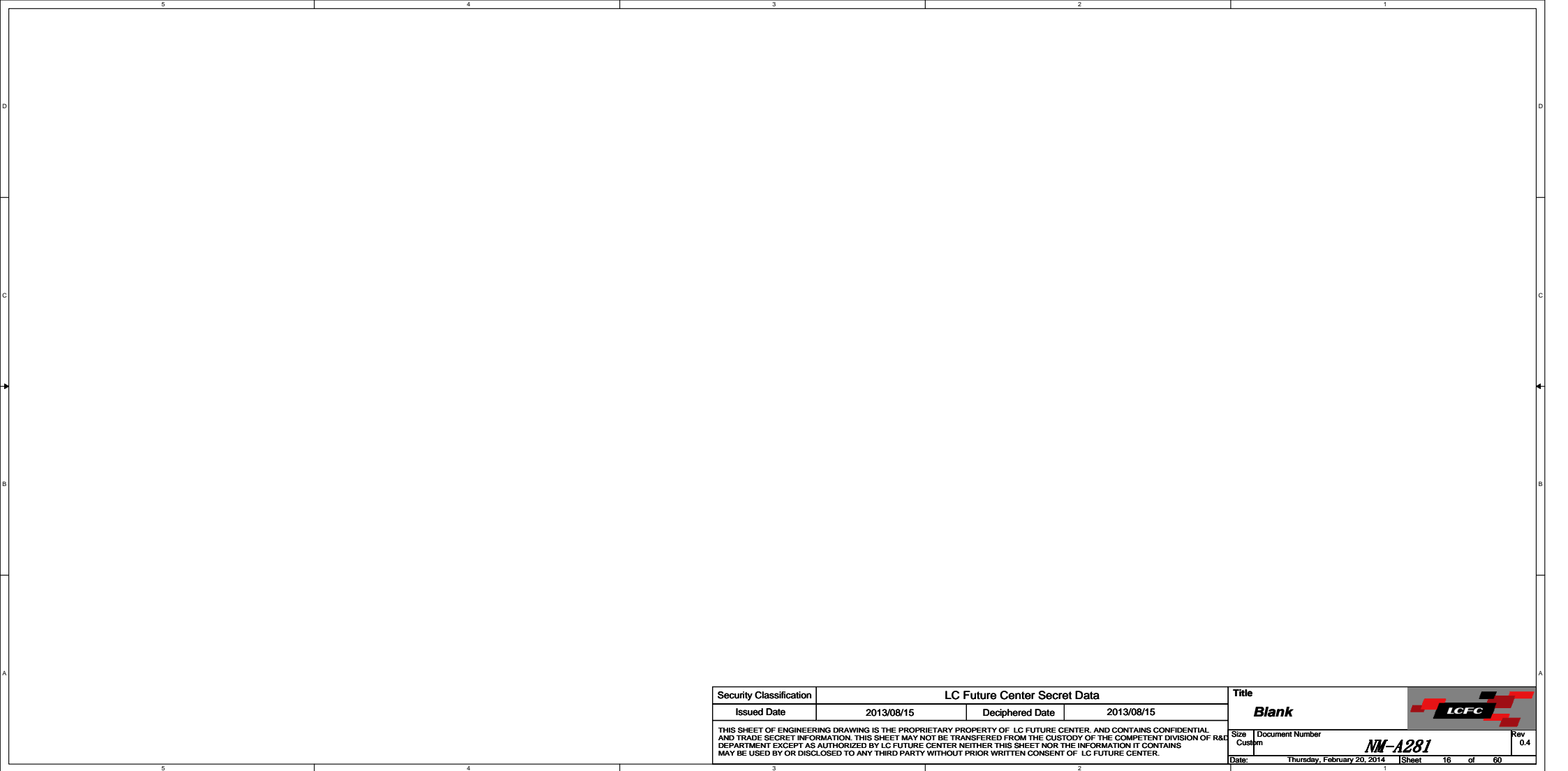



Layout Note:
Place near DIMM

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VGA Note list need to be update!

Power-Up/Down Sequence

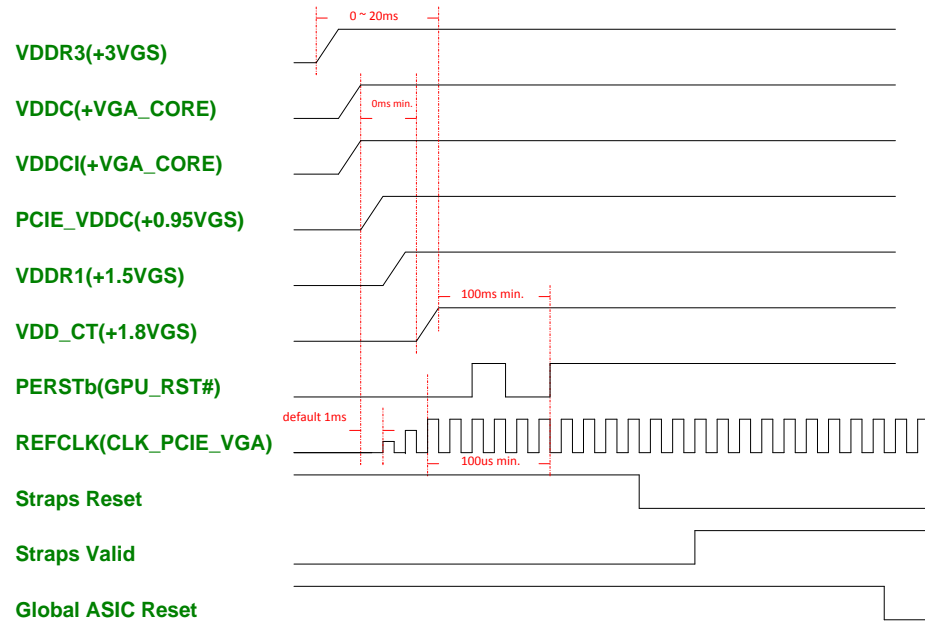
"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.

The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.

VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).

For power down, reversing the ramp-up sequence is recommended.

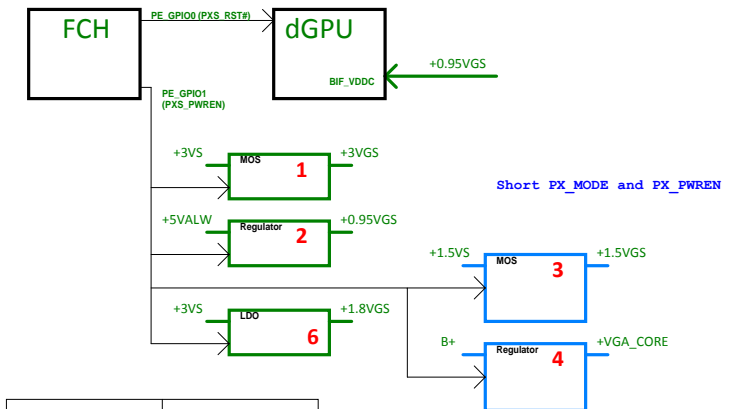


Without BACO option :

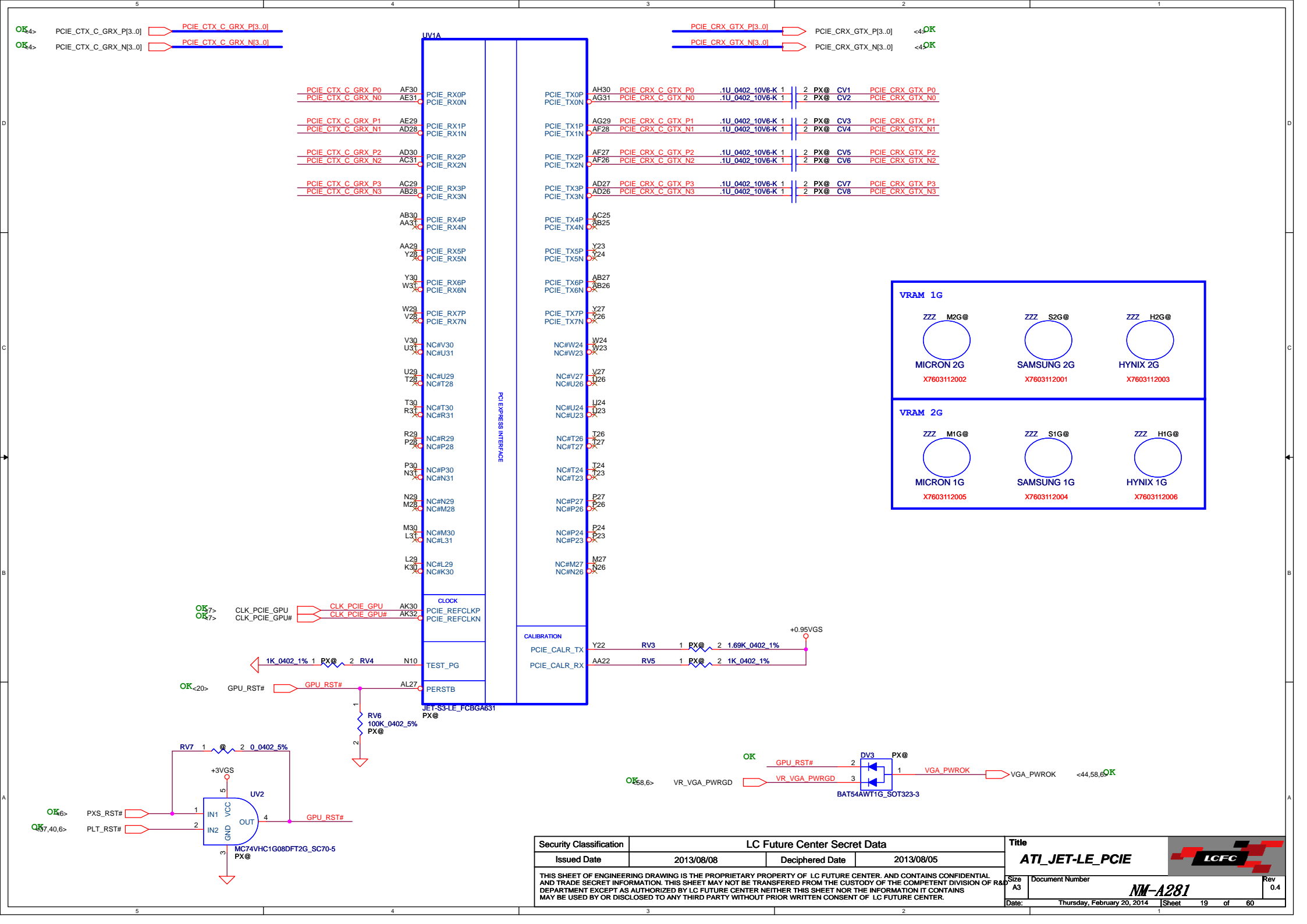
PE_GPIO0 : Low -> Reset dGPU ; High -> Normal operation
 PE_GPIO1 : Low -> dGPU Power Off ; High -> dGPU Power ON

dGPU Power Pins	Voltage	Max current
VDD_CT, DP_VDDR, SPLL_PVDD, MPLL_PVDD, PCIE_PVDD, TSVDD, VDDR4, AVDD, VDD1D1	1.8V	1243mA
DP_VDDC, SPLL_VDDC, PCIE_VDDC, BIF_VDDC	0.95V	4560mA
VDDR3	3.3V	25mA
VDDR1	1.5V	1.5A
VDDC	0.8~1.125V	TBD
VDDCI	0.8~1.1V	8.8A

PX5.5

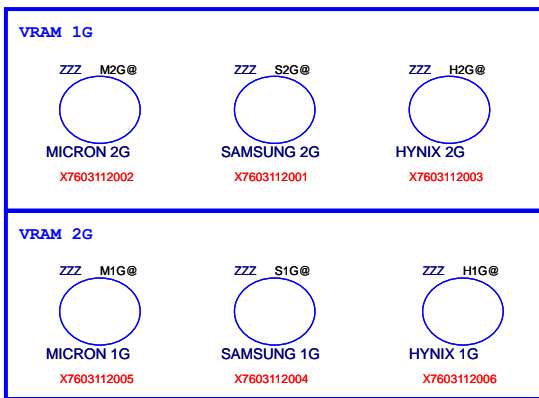
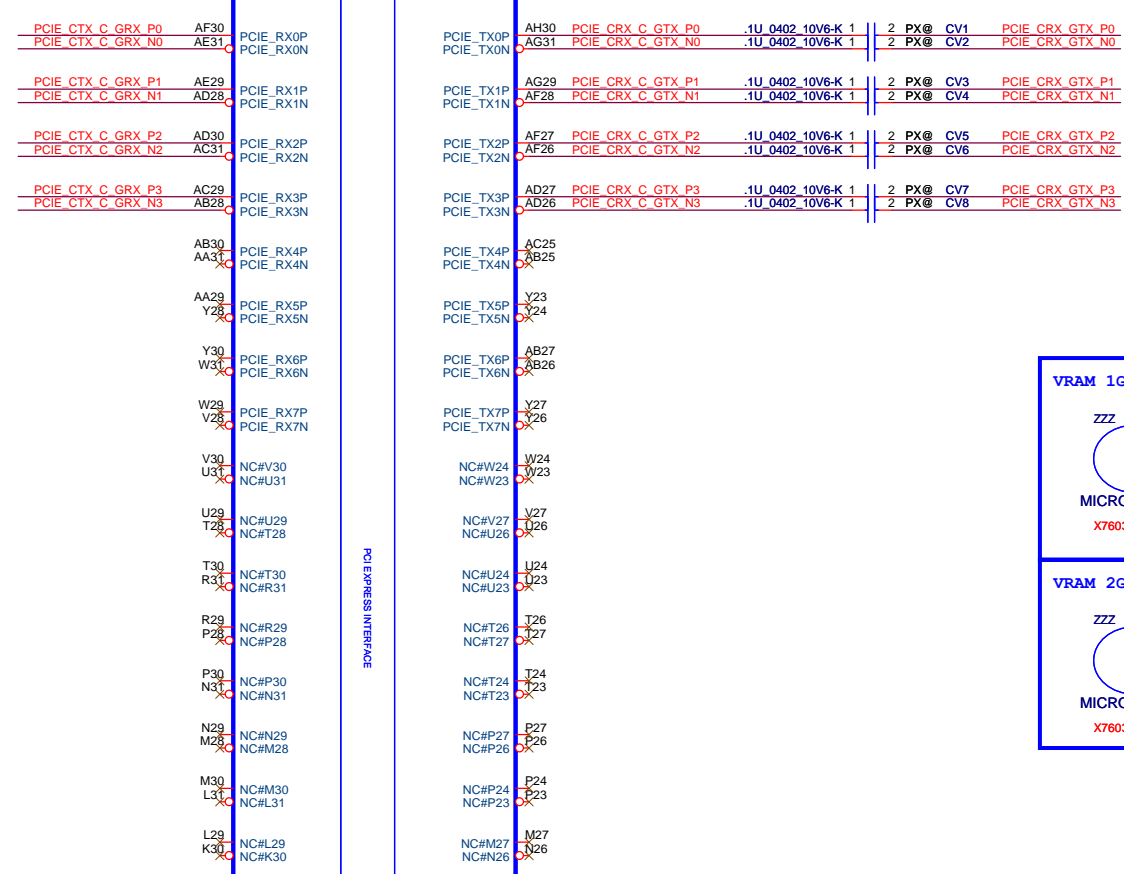


Name	Pin Assignment
PE_GPIO0	GPIO191
PE_GPIO1	GPIO192



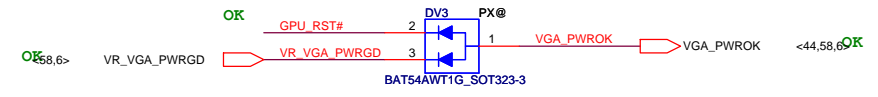
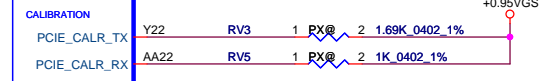
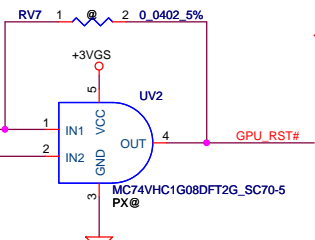
OK4> PCIE_CTX_C_GRP_P[3..0] → PCIE_CTX_C_GRP_P[3..0]
 OK4> PCIE_CTX_C_GRP_N[3..0] → PCIE_CTX_C_GRP_N[3..0]

PCIE_CRX_GTX_P[3..0] → PCIE_CRX_GTX_P[3..0] <4>OK
 PCIE_CRX_GTX_N[3..0] → PCIE_CRX_GTX_N[3..0] <4>OK

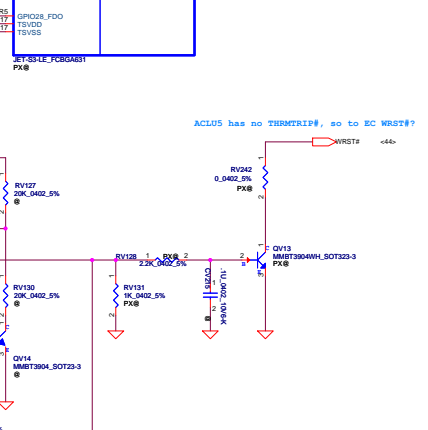
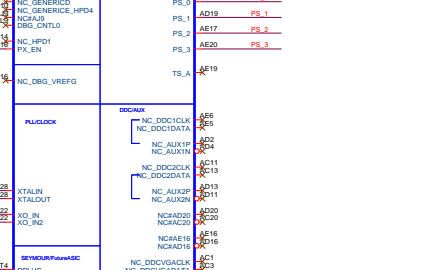
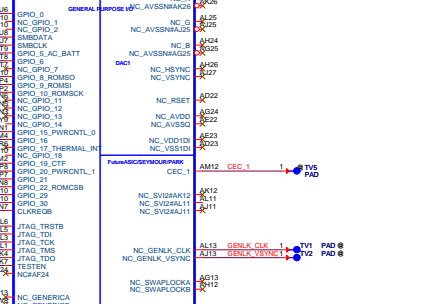
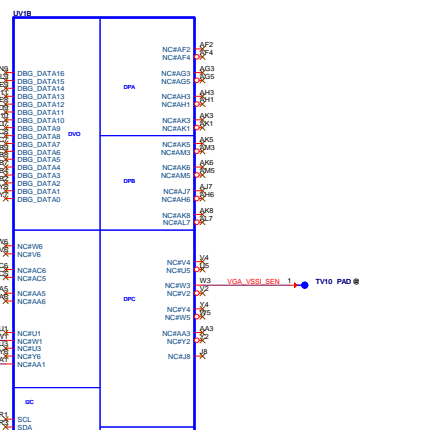
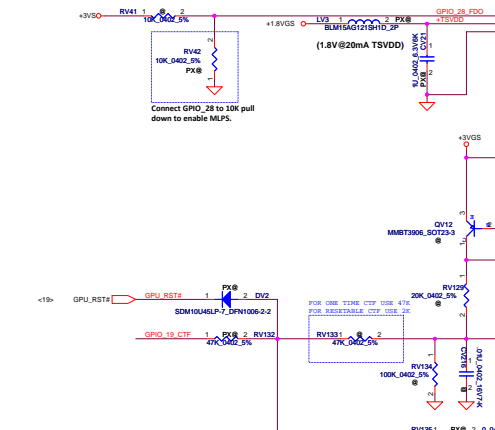
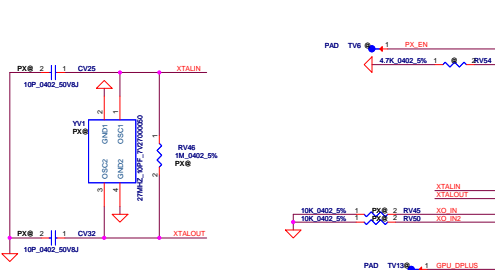
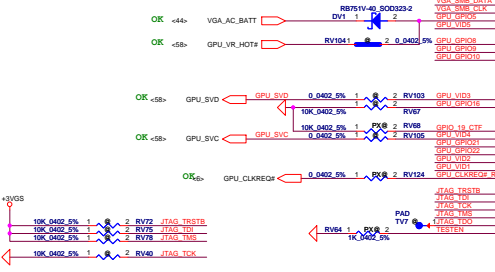
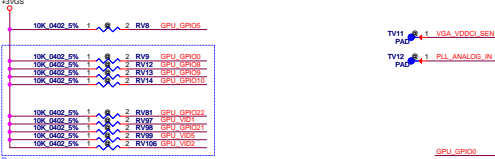
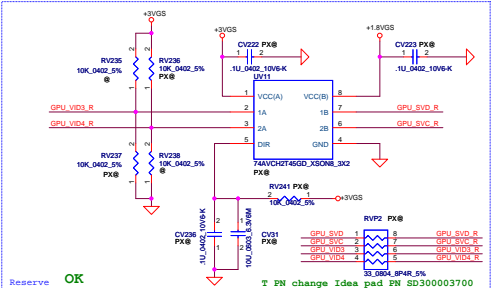


OK7-> CLK_PCIE_GPU AK30
 OK7-> CLK_PCIE_GPU# AK32

OK<20> GPU_RST# → GPU_RST#

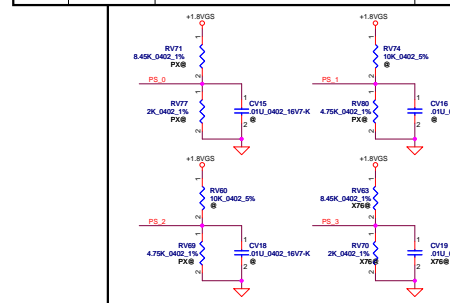


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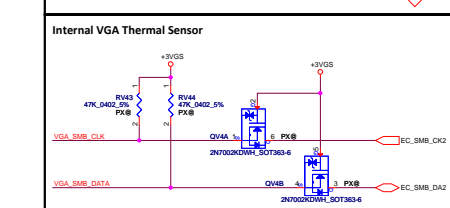
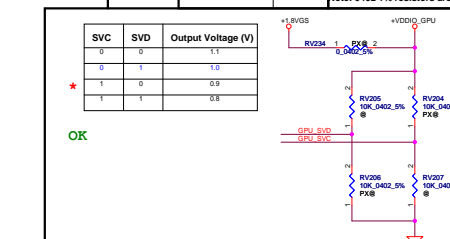


CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

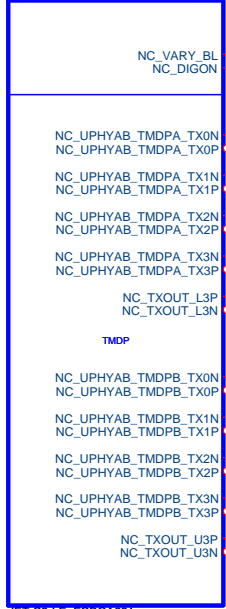
MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_[0]	ROM_CONFIG[0]	Define the ROM type when STRAP_BIOS_ROM_EN = 1	
PS_[0]	ROM_CONFIG[1]	Define the primary memory structure size when STRAP_BIOS_ROM_EN = 0.	100 = 256MB
PS_[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_[6]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	X
PS_[11]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported 0 = PCIe GEN3 is not supported	0 = Not support
PS_[12]	STRAP_BIF_CLK_PMEN	0 = The CLKREQ power management capability is disabled 1 = The CLKREQ power management capability is enabled	0
PS_[13]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_[14]	STRAP_TX_CPD_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_[16]	STRAP_TX_DEEMPHLEN	0 = Tx deemphases disabled 1 = Tx deemphases enabled.	1 = Enable
PS_[21]	N/A	Reserved.	NA
PS_[22]	N/A	Reserved.	NA
PS_[23]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable
PS_[24]	STRAP_BIF_VGA_DIS	0 = VGA controller capability enabled. 1 = The device will not be recognized as the system's VGA controller.	0
PS_[26]	N/A	Reserved.	NA
PS_[31]	BOARD_CONFIG[0]	Board configuration related strap options such as for memory ID	X
PS_[31]	BOARD_CONFIG[1]	110 = Hynix 1G 111 = Micron 1G 112 = Samsung 1G	
PS_[31]	BOARD_CONFIG[2]	000 = No usable endpoints 001 = One usable endpoint 010 = Two usable endpoints 011 = Three usable endpoints 011 = Four usable endpoints 010 = Five usable endpoints 001 = Six usable endpoints 000 = All endpoints are usable.	X
PS_[34]	AUD_PORT_CONN_PINSTRAP[1]	Determines the maximum number of digital display audio endpoints that will be generated for the OS and user. (Combine with PS_[35])	
PS_[35]	AUD_PORT_CONN_PINSTRAP[0]	111 = No usable endpoints 110 = One usable endpoint 101 = Two usable endpoints 100 = Three usable endpoints 011 = Four usable endpoints 010 = Five usable endpoints 001 = Six usable endpoints 000 = All endpoints are usable.	X



MLPS	BLT				BOM			
	5	4	3	2	1	R_pu (Ω)	R_pd (Ω)	C (nF)
PS_0 [5:1]	1	1	0	0	0	RV71=8.45k	RV77=2k	CV15=NC
PS_1 [5:1]	1	1	0	0	0	RV74=NC	RV90=4.75k	CV16=NC
PS_2 [5:1]	1	1	0	0	0	RV77=4.75k	RV78=4.75k	CV18=NC
PS_3 [5:1]	1	1	1	1	1	RV60=NC	RV69=4.75k	CV19=NC
PS_3 [5:1]	1	1	1	1	1	RV60=NC	RV69=4.75k	CV19=NC




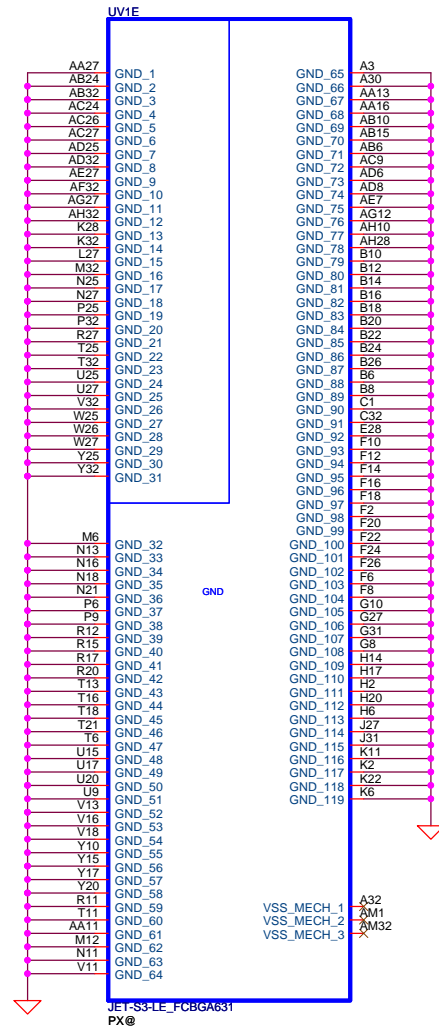
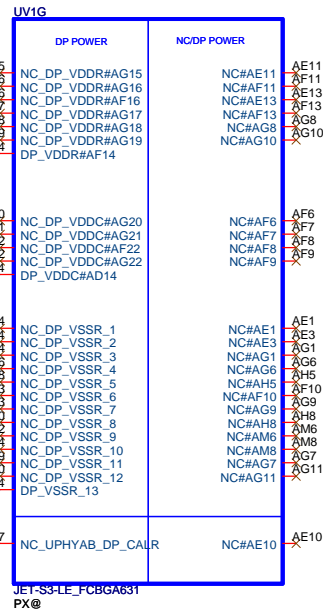
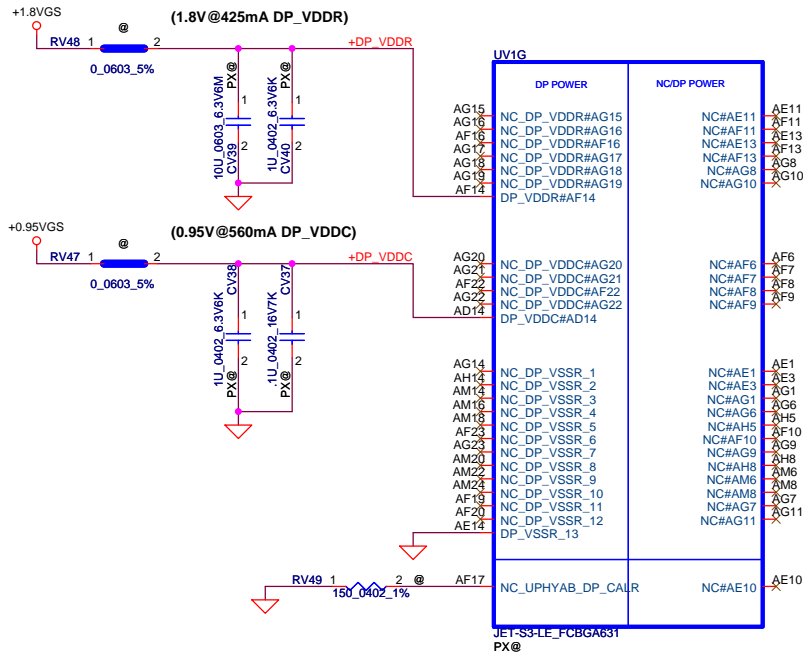
UV1F



JET-S3-LE_FCBGA631
PX@

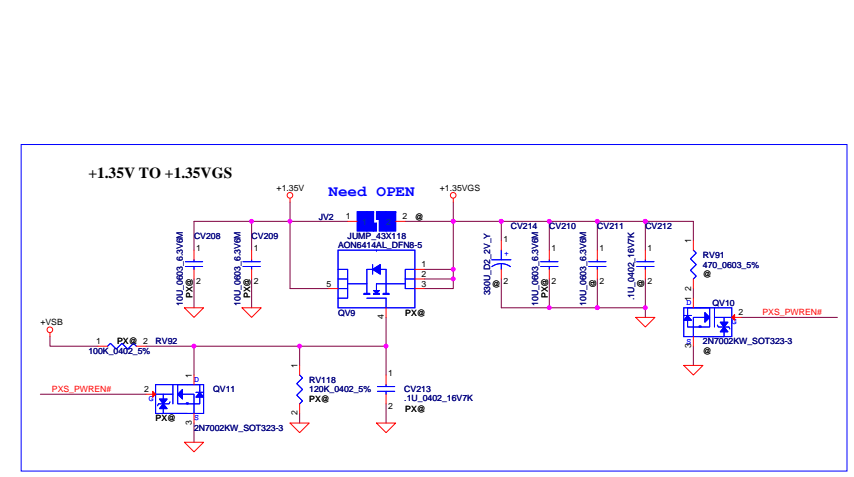
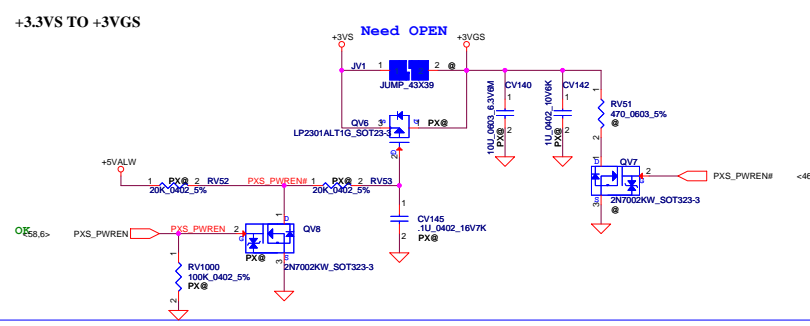
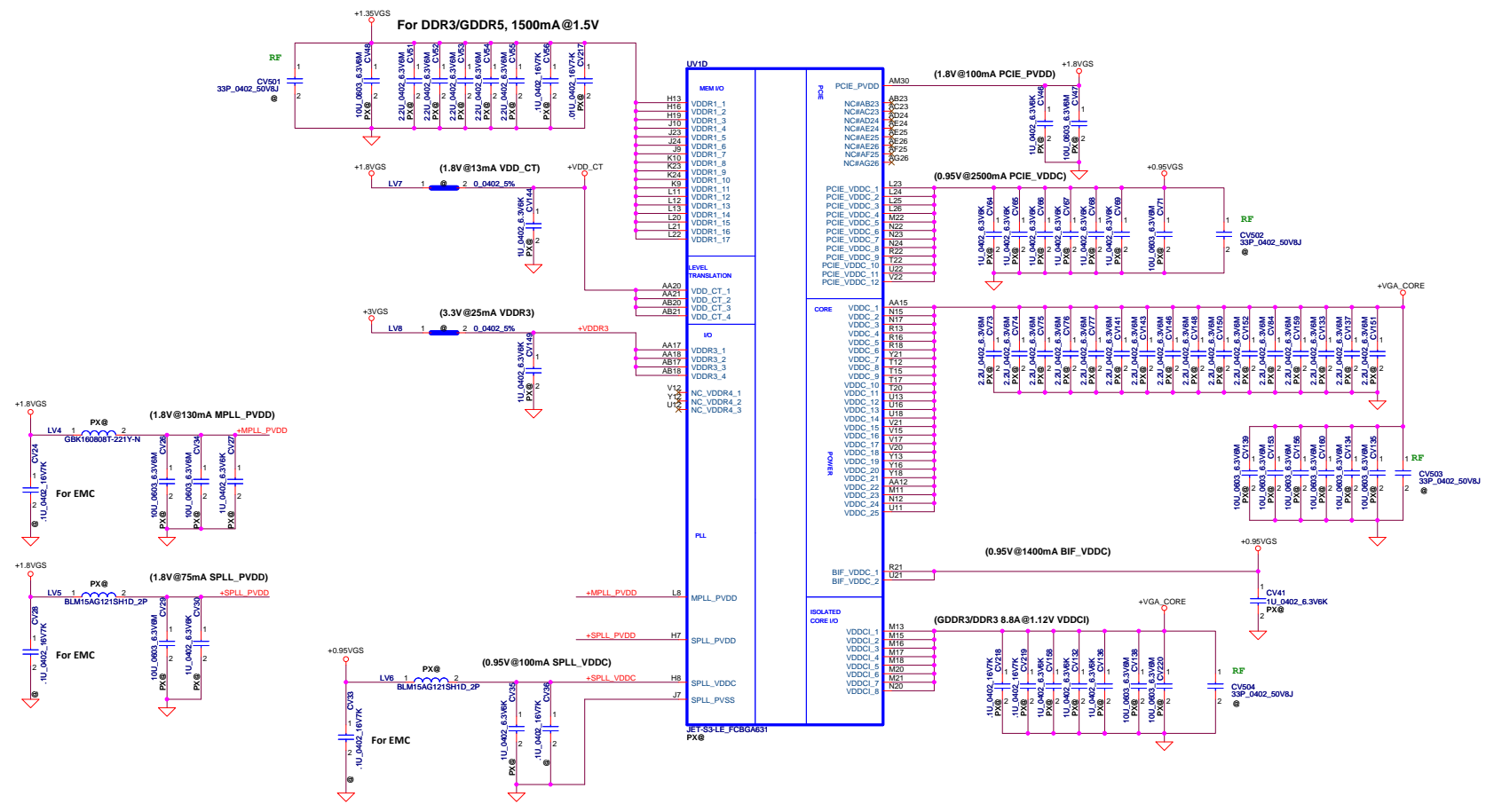
- AB11
- AB12
- AL15
- AK14
- AH16
- AJ15
- AL17
- AK16
- AH18
- AJ17
- AL19
- AK18
- AH20
- AJ19
- AL21
- AK20
- AH22
- AJ21
- AL23
- AK22
- AK24
- AJ23

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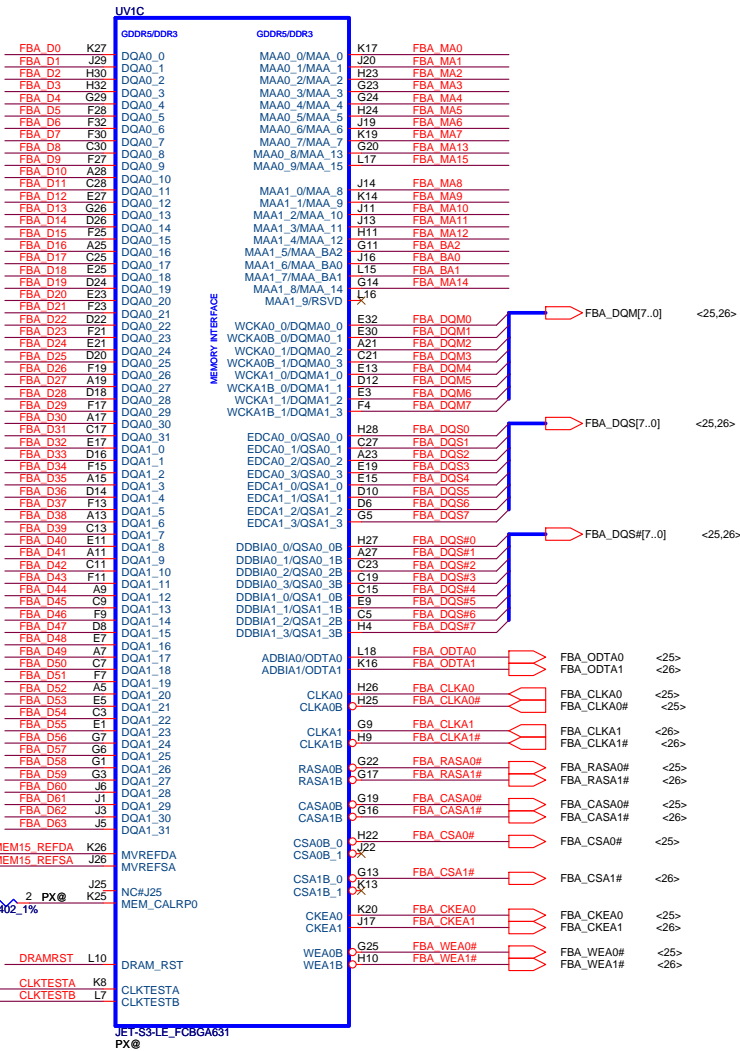
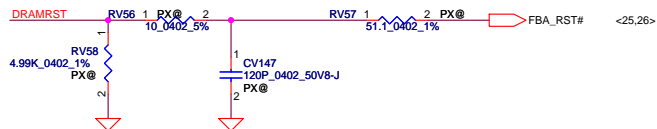
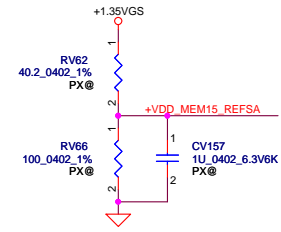
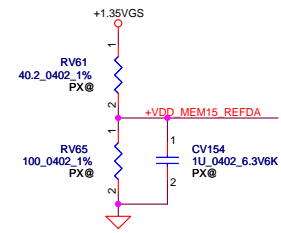
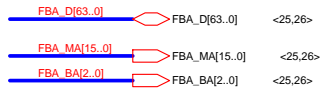


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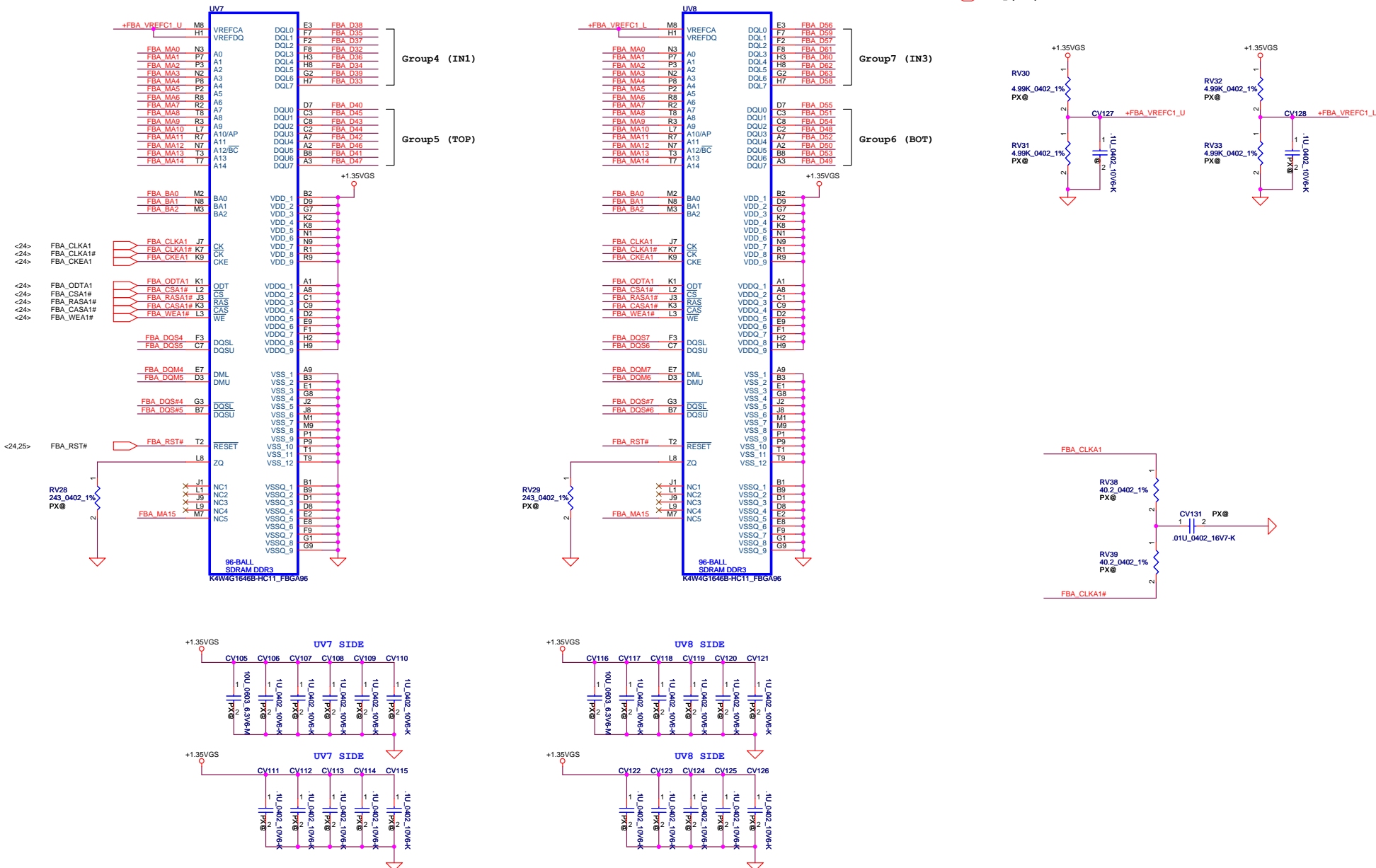



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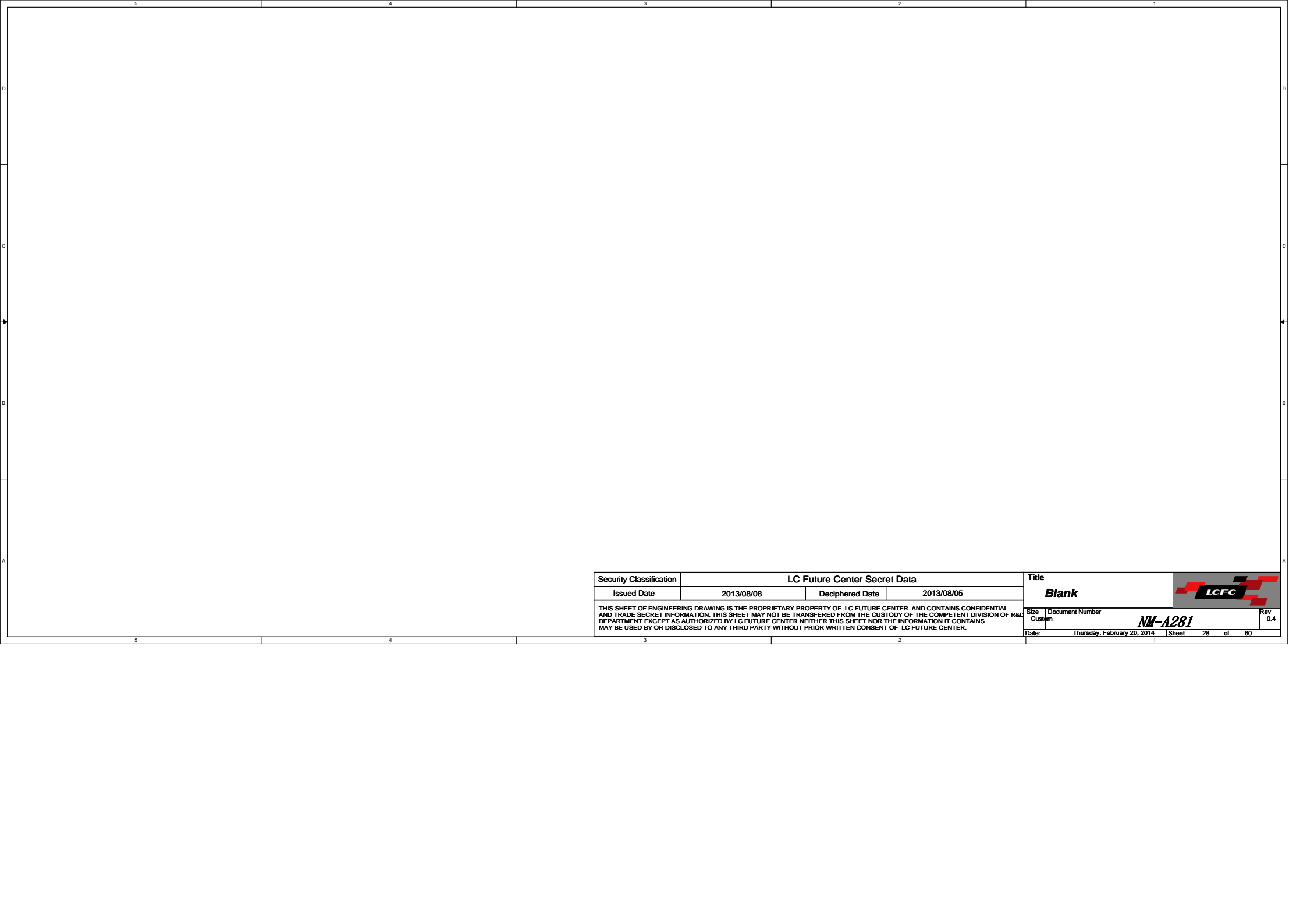



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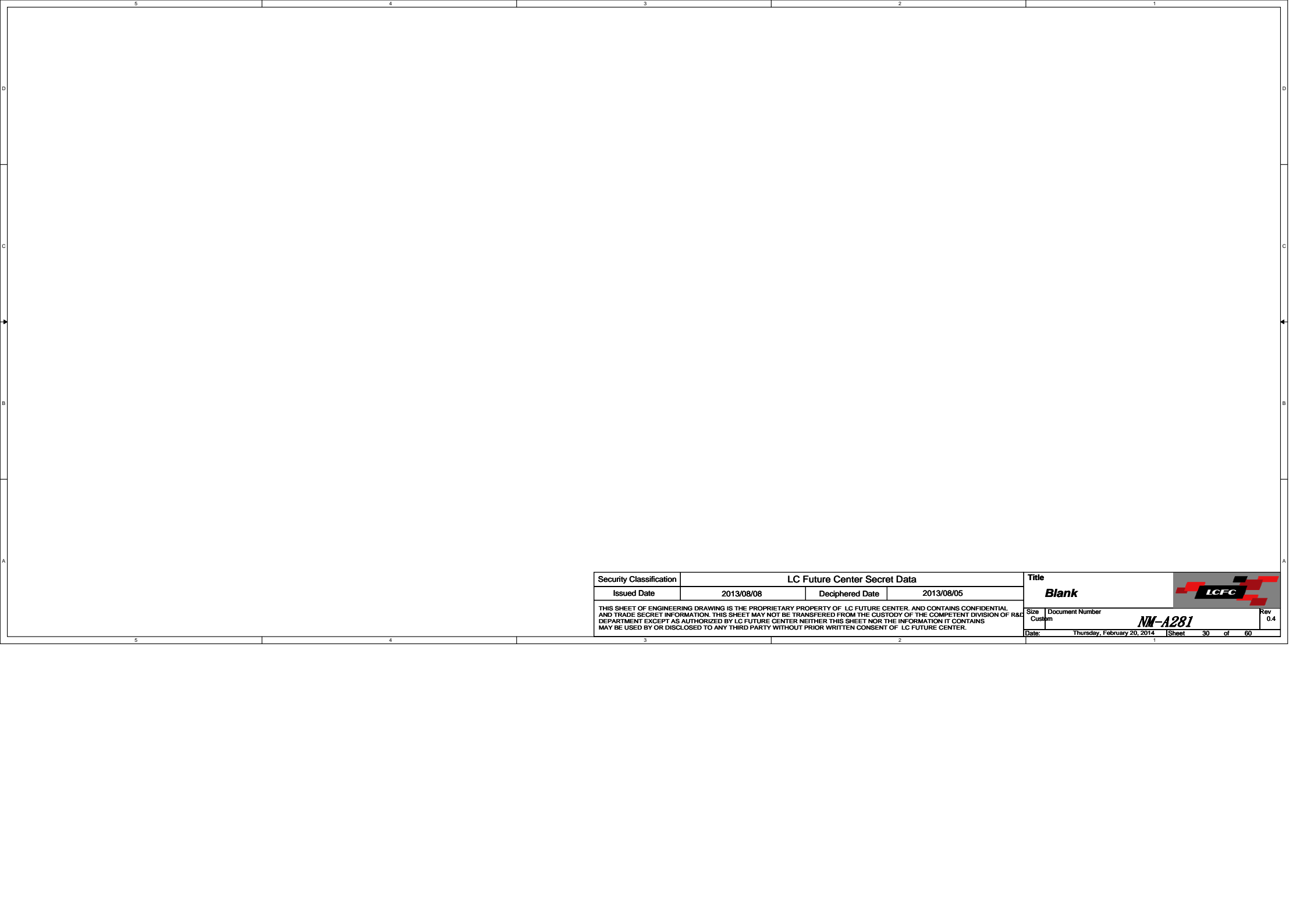
Memory Partition A - Upper 32 bits




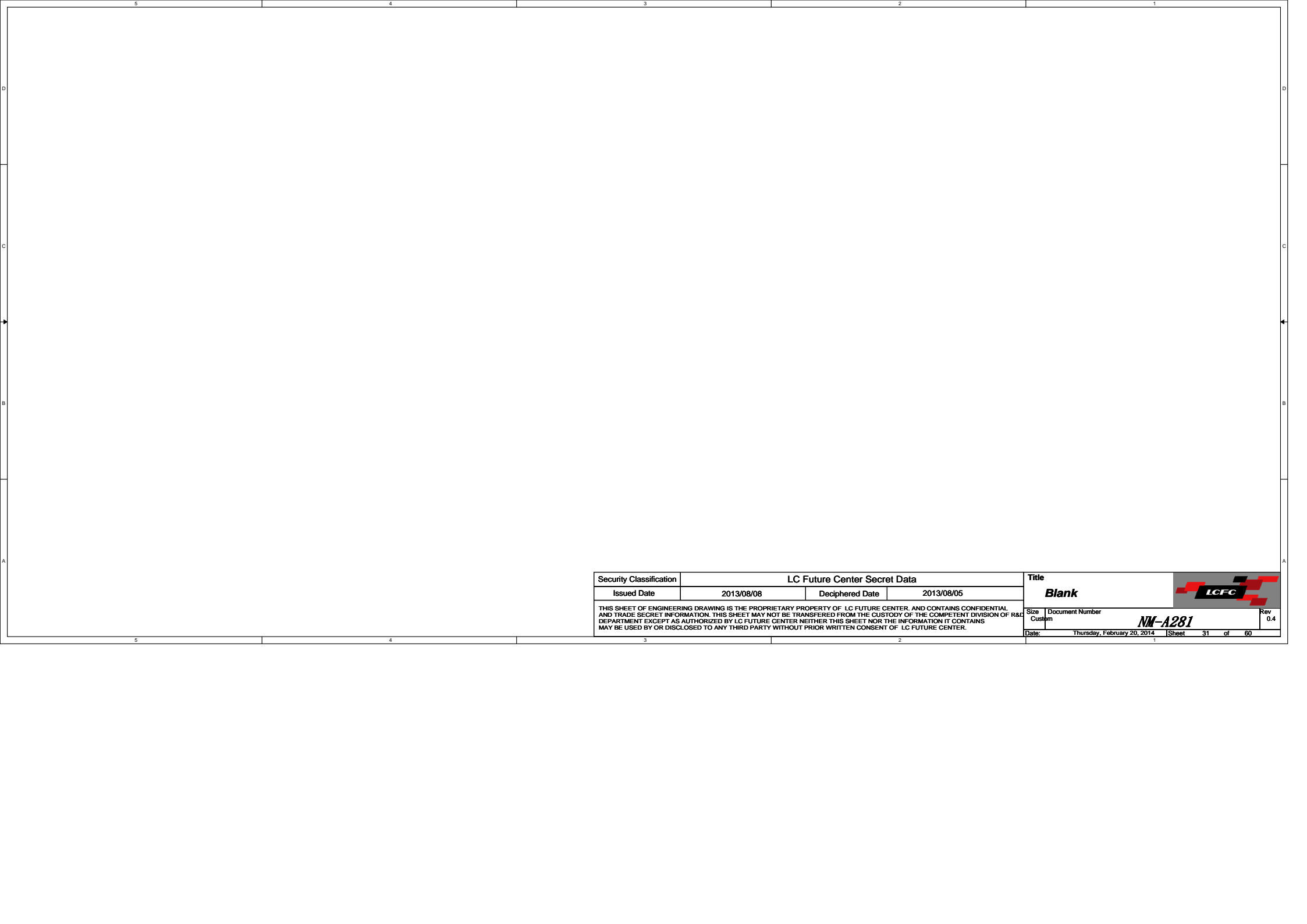
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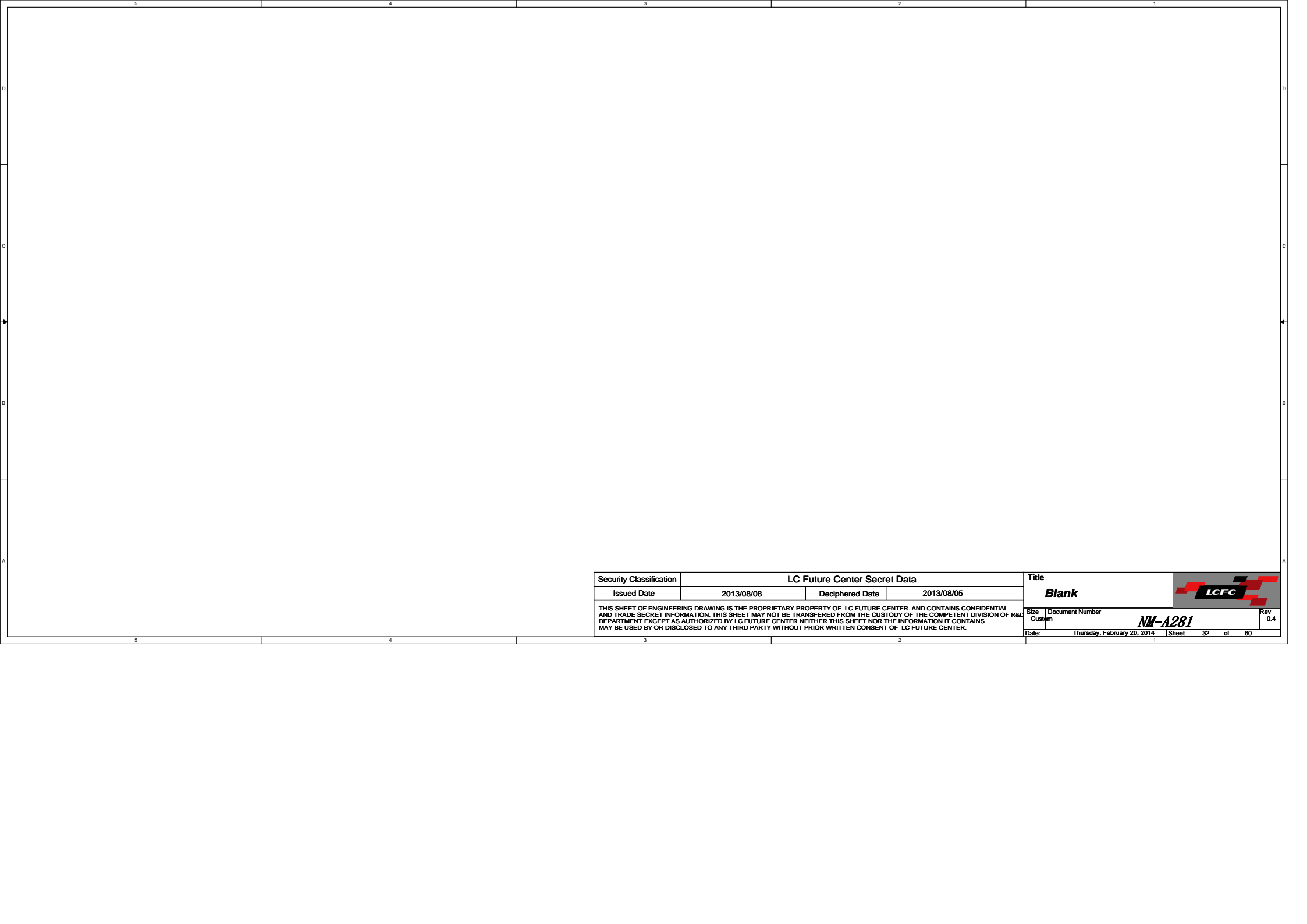
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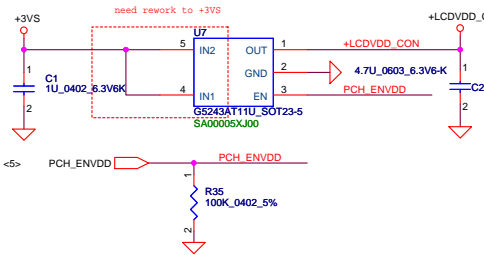


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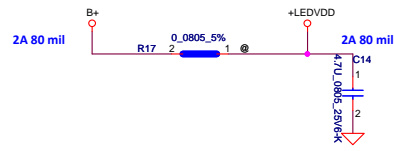


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LCD POWER CIRCUIT OK

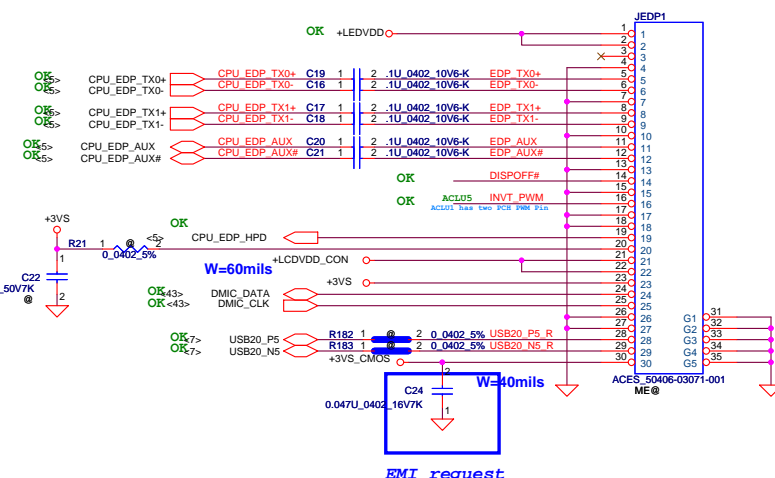
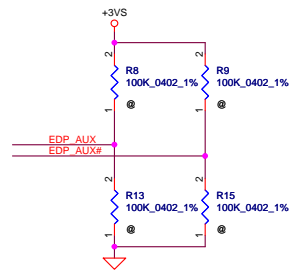
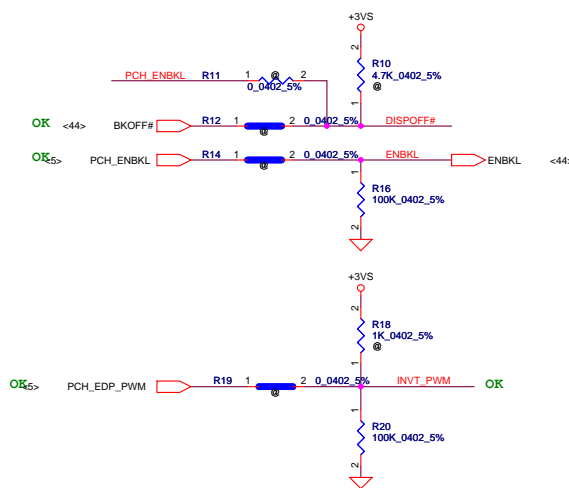
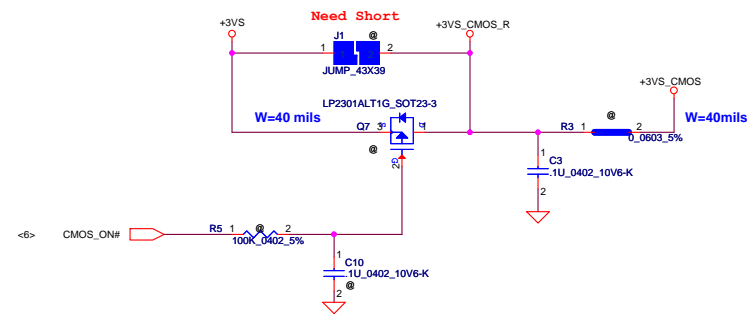


B+ to +LEDVDD POWER OK

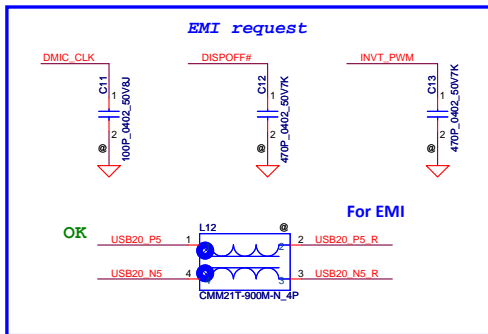
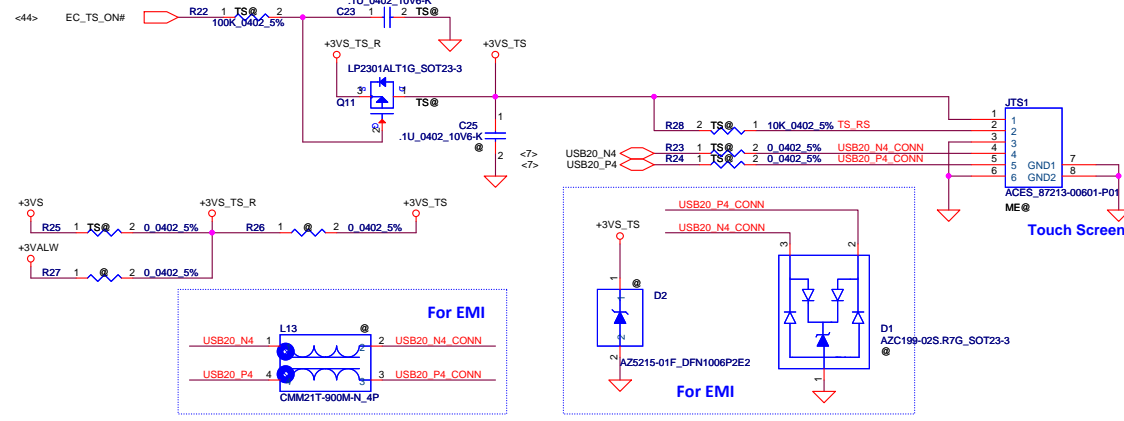


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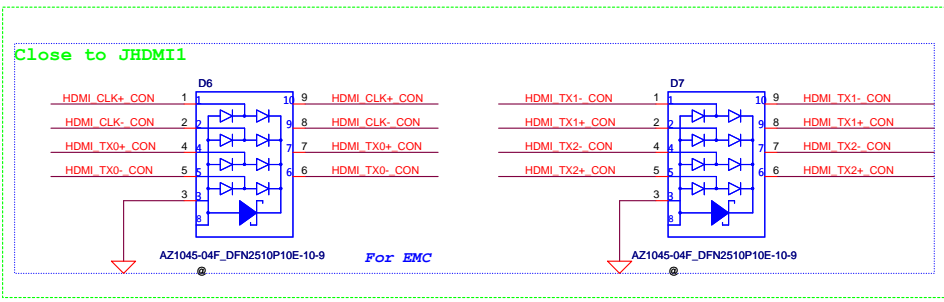
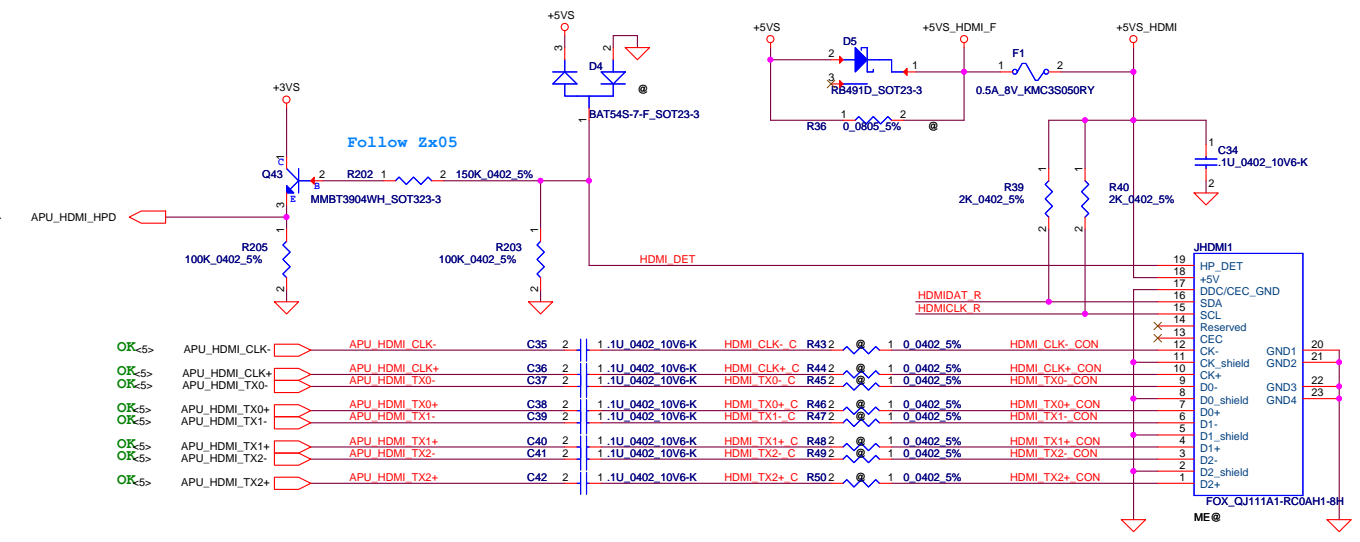
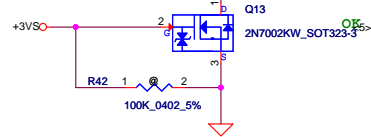
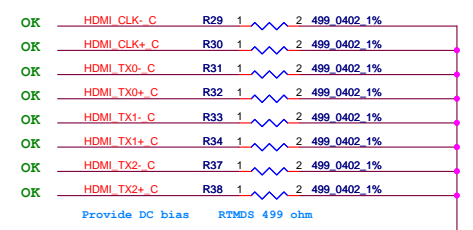
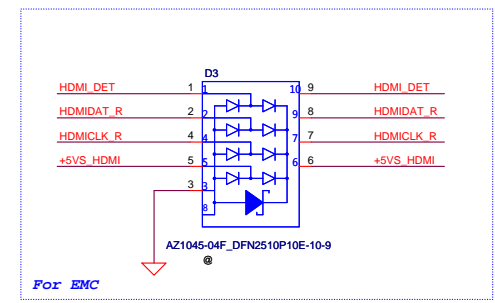
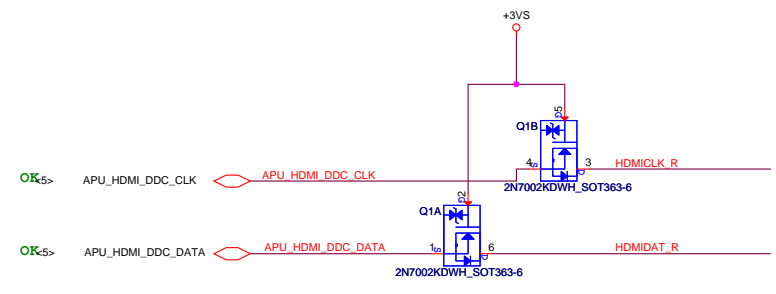
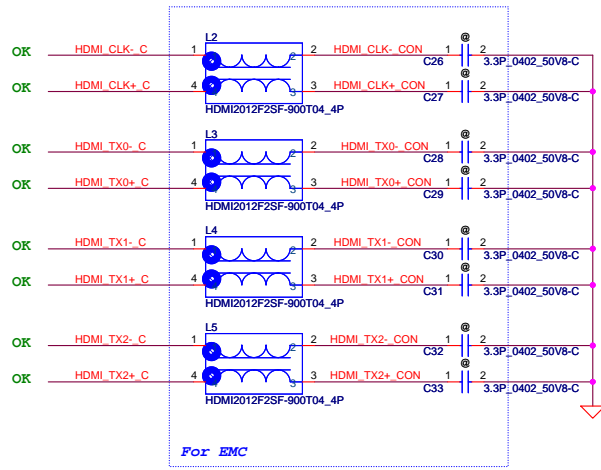
CMOS Camera



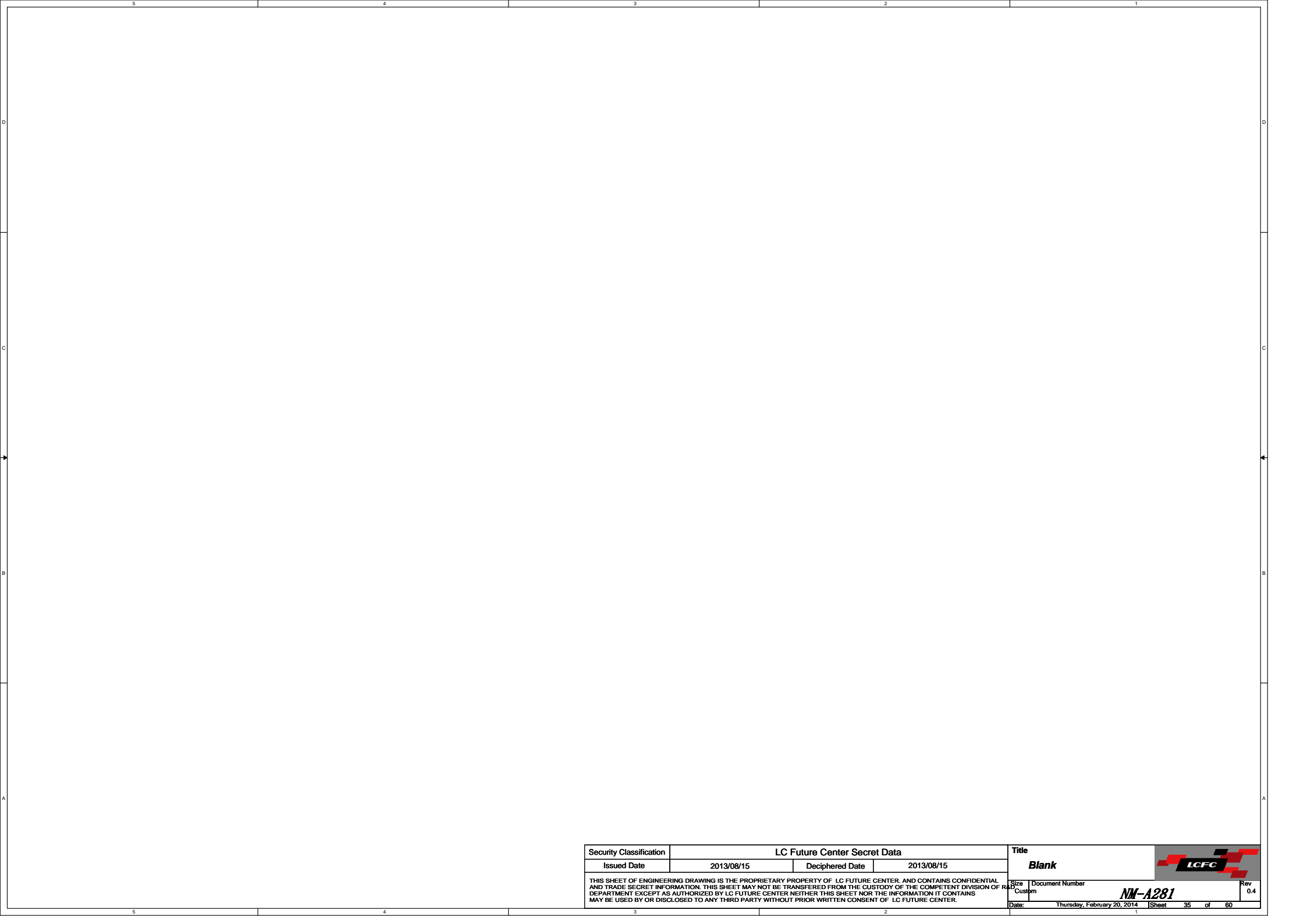
Touch Screen OK




Security Classification	LC Future Center Secret Data		Title	eDP/ CMOS/Touch screen
Issued Date	2013/08/08	Deciphered Date	2013/08/05	
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Size	Document Number	Date		Rev
Custom	NM-A281	Thursday, February 20, 2014 11:58 AM		0.4
			Sheet	33 of 60

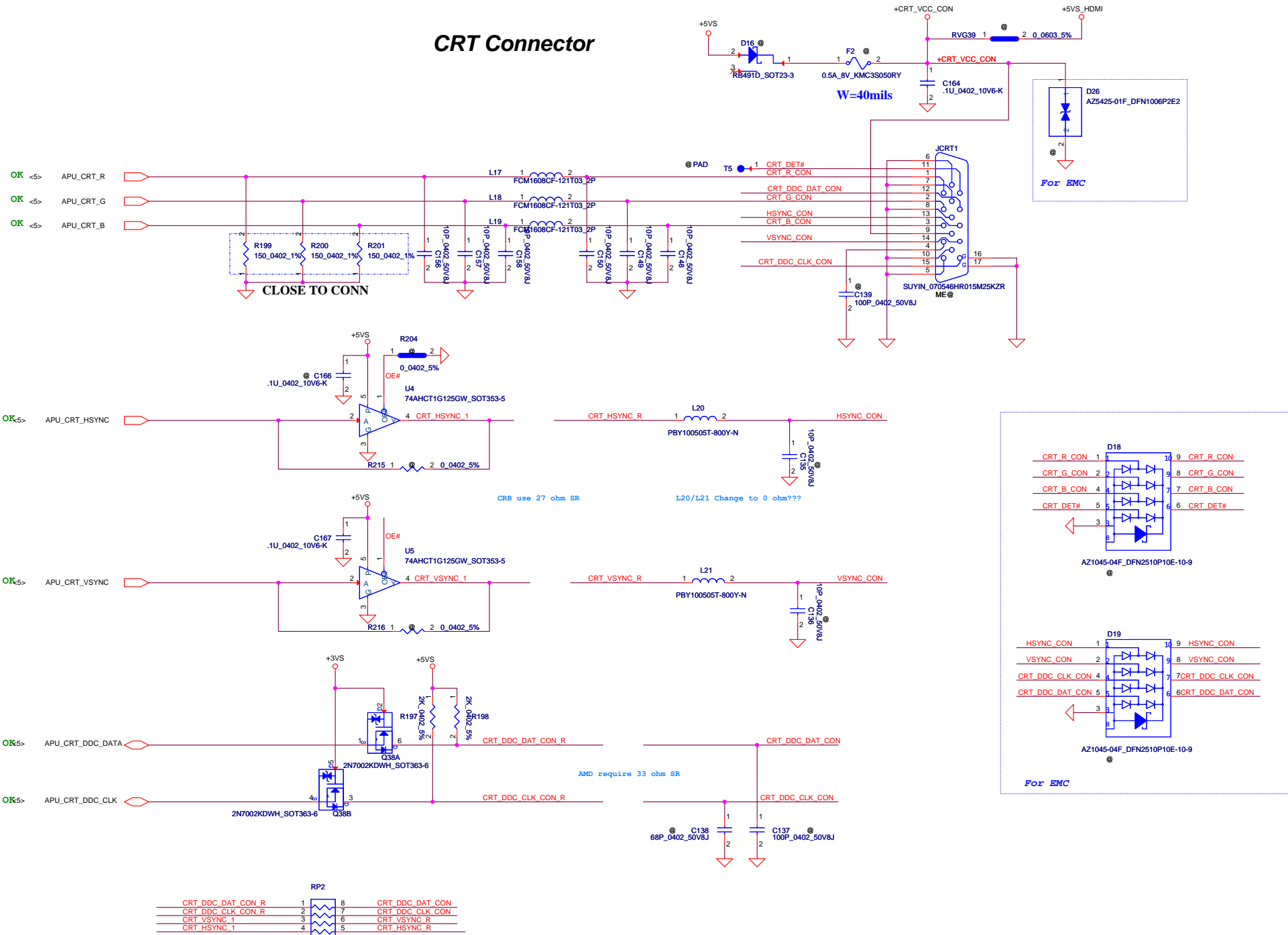


Security Classification		LC Future Center Secret Data		Title		
Issued Date	2013/08/15	Deciphered Date	2013/08/15	HDMI_CONN		
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Date:	Thursday, February 20, 2014	Sheet	34	of	60	Rev 0.4 NM-A281

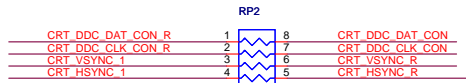


Security Classification	LC Future Center Secret Data			Title	
Issued Date	2013/08/15	Deciphered Date	2013/08/15	Blank	
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				Date: Thursday, February 20, 2014	Rev 0.4
				Sheet 35 of 60	

CRT Connector



T PN change Idea pad PN SD300003700

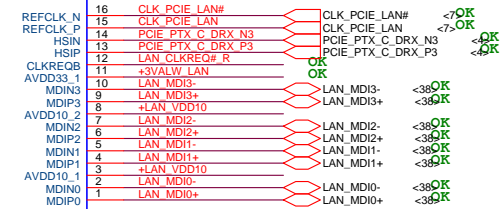
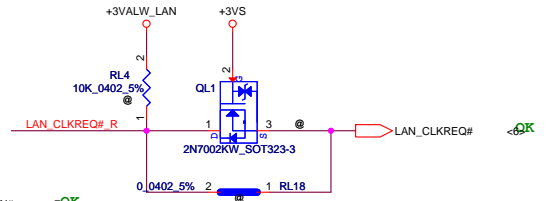
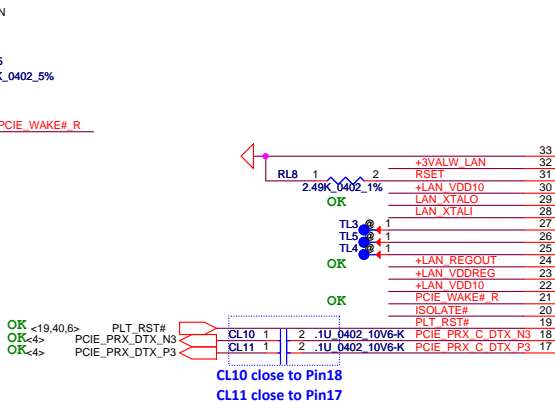
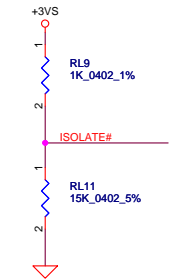
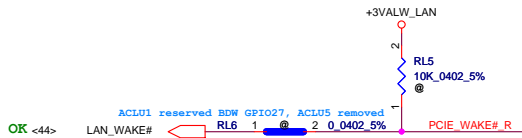
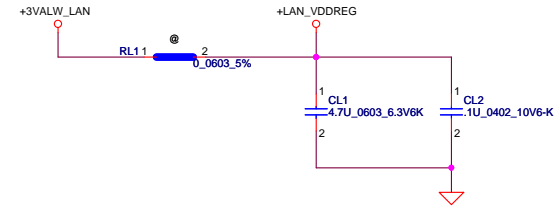
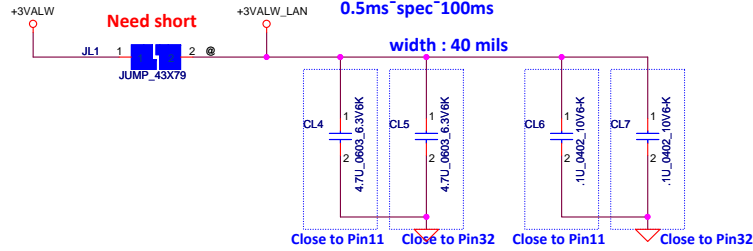


Security Classification		LC Future Center Secret Data	
Issued Date	2013/08/15	Deciphered Date	2013/08/15
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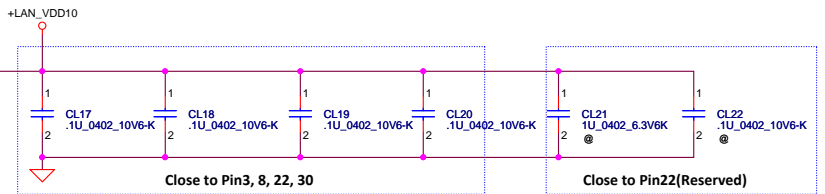
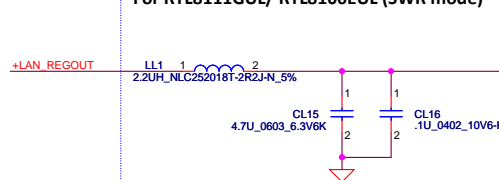
Title		LCFC	
CRT		Size	Rev
Custom	Document Number	NM-A281	0.4
Date:	Thursday, February 20, 2014	Sheet	36 of 60

+3VALW TO +3VALW_LAN

+3VALW_LAN rising time (10%~90%):
0.5ms spec~100ms

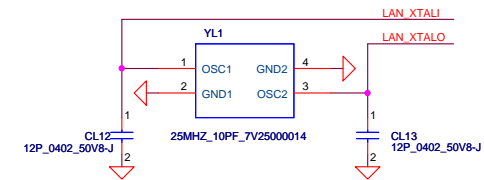


For RTL8111GUL/RTL8106EUL (SWR mode)



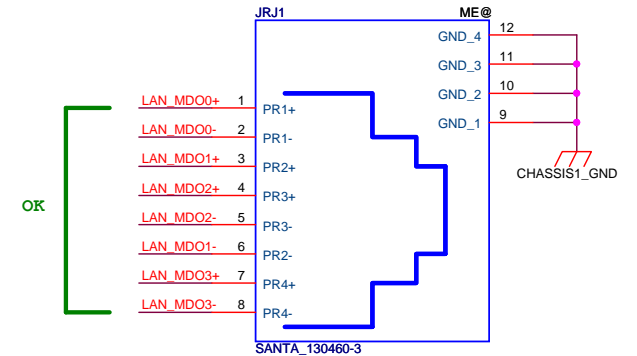
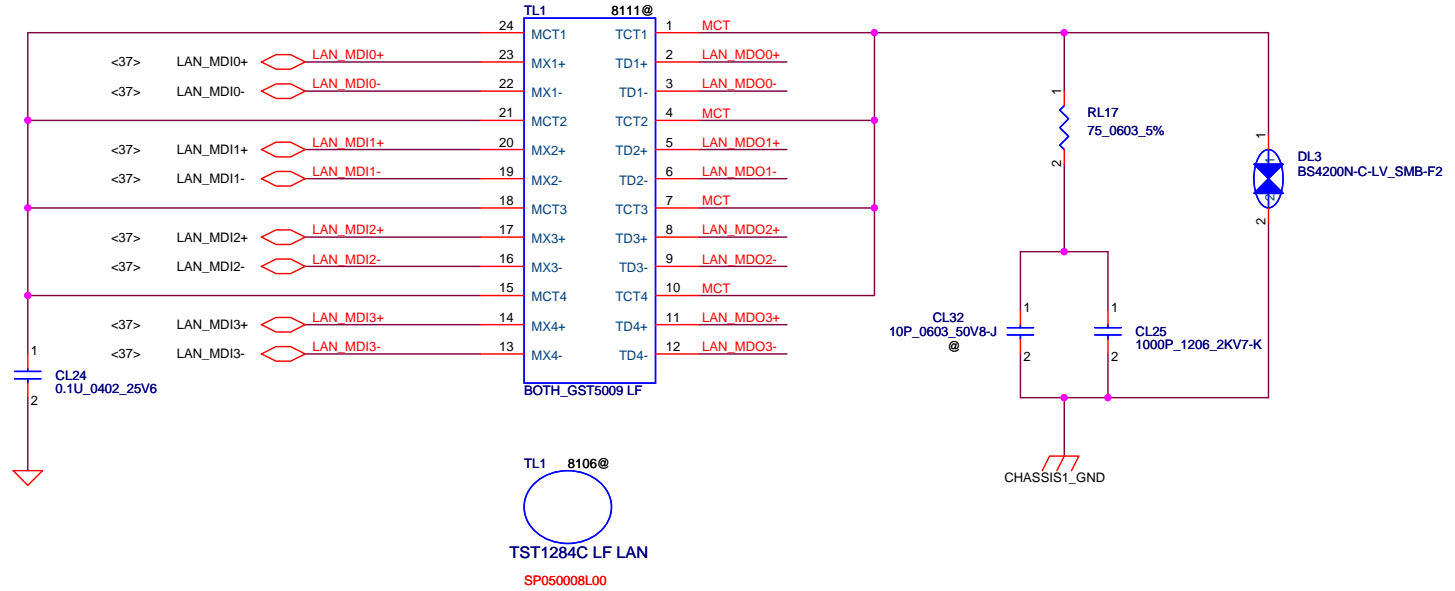
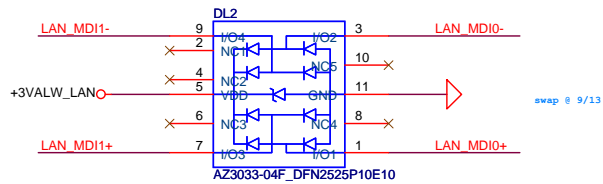
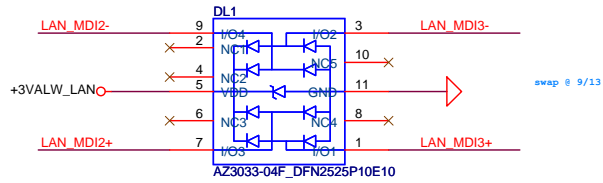
Layout Note: LL1 must be within 200mil to Pin36,
CL15,CL16 must be within 200mil to LL1
+LAN_REGOUT: Width =60mil

LAN ROM OK



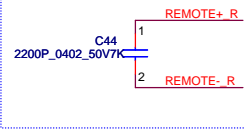
Security Classification		LC Future Center Secret Data		Title	
Issued Date	2013/08/08	Deciphered Date	2013/08/05	LAN_RTL8111GUL/RTL8106E	
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	NM-A281	Thursday, February 20, 2014		Sheet	37 of 60

DL1/DL2
1'S PN:SC30003M00



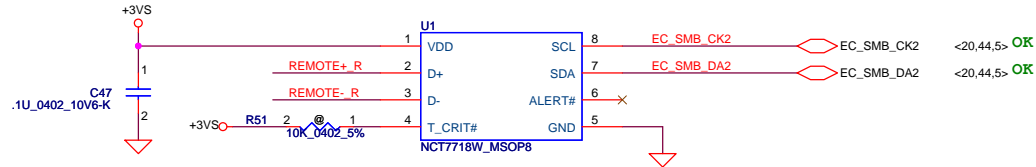
Security Classification	LC Future Center Secret Data			Title	LAN Transformer
Issued Date	2013/08/08	Deciphered Date	2013/08/05	Document Number	
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Close to U1

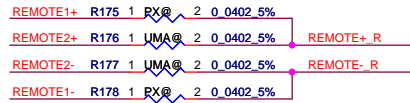
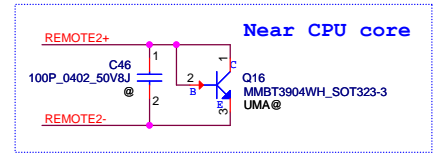
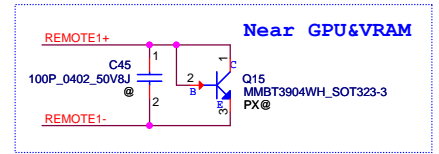


SMSC thermal sensor placed near DIMM

OK

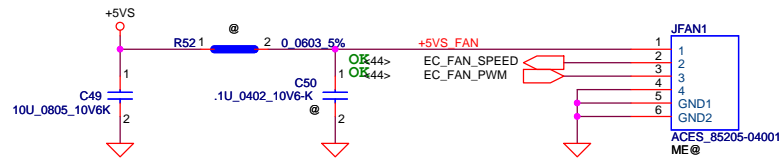


Address 1001_101xb



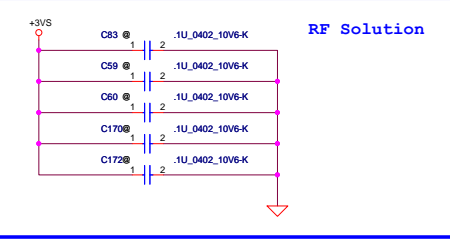
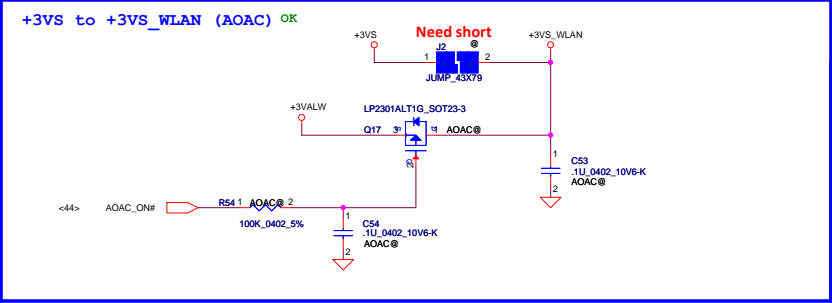
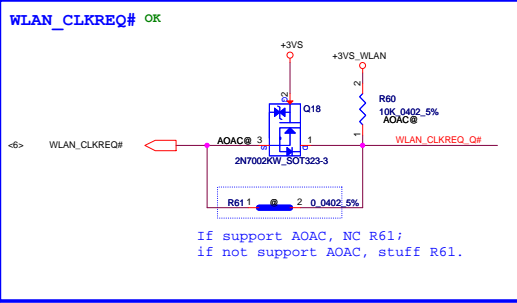
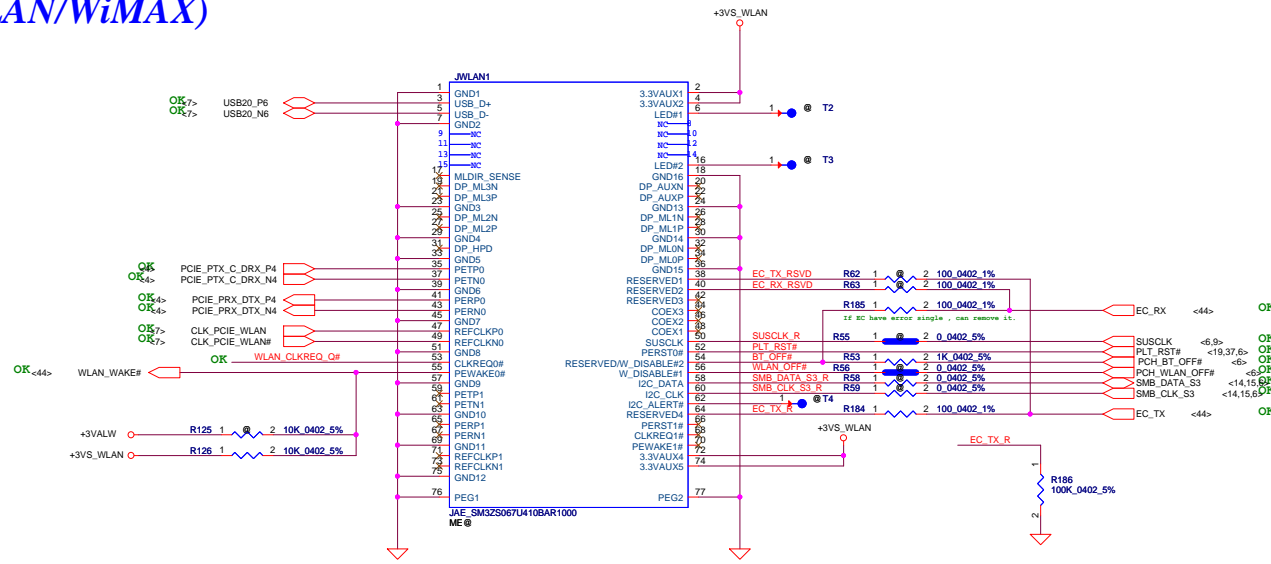
REMOTE+/-_R, REMOTE1+/-, REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN Conn

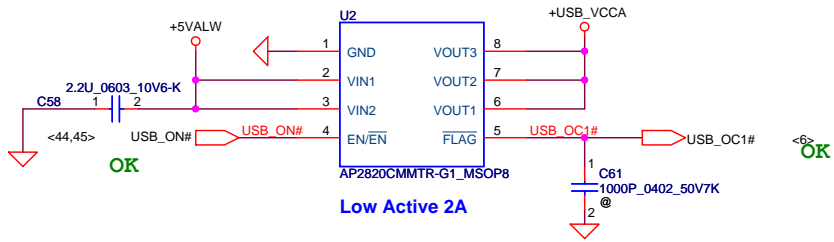


Security Classification	LC Future Center Secret Data		Title	
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Size	Document Number	Date:		Rev
Custom	NM-A281	Thursday, February 20, 2014		0.4
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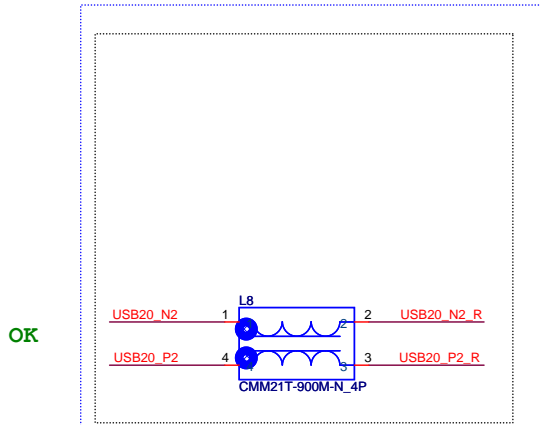
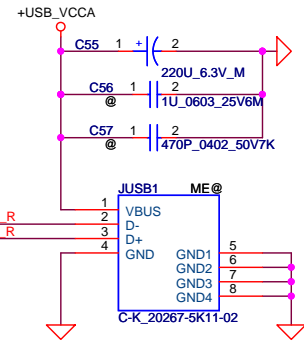
Mini-Express Card(WLAN/WiMAX)



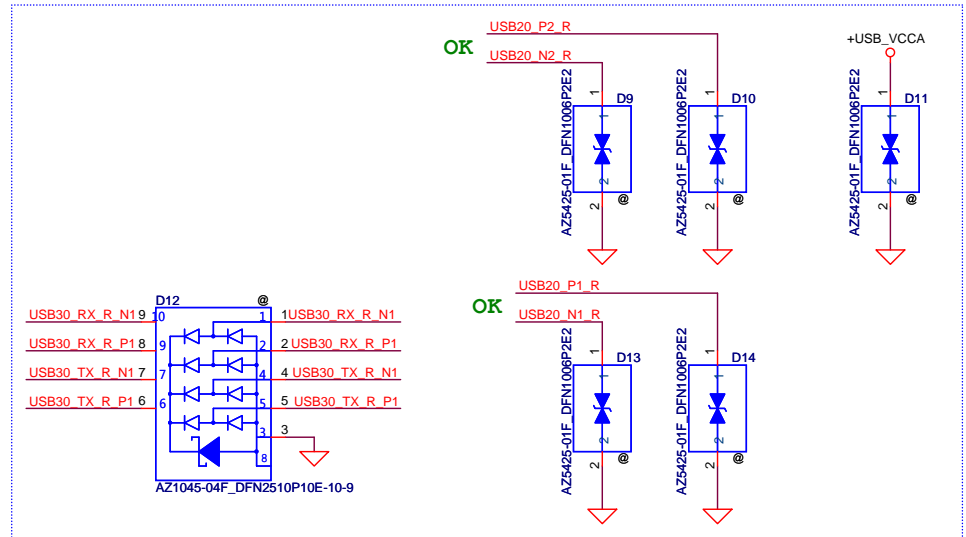
LEFT SIDE USB3.0 PORT X2



OK <7>

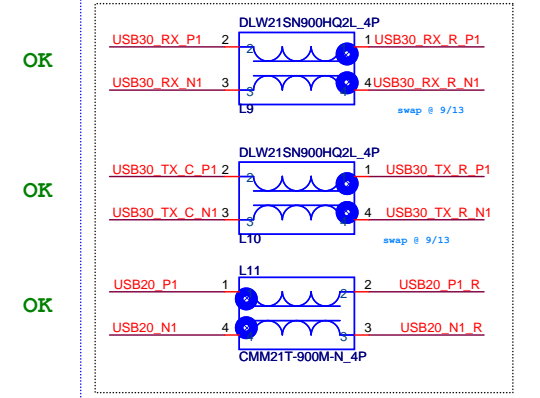


OK



OK

For EMC

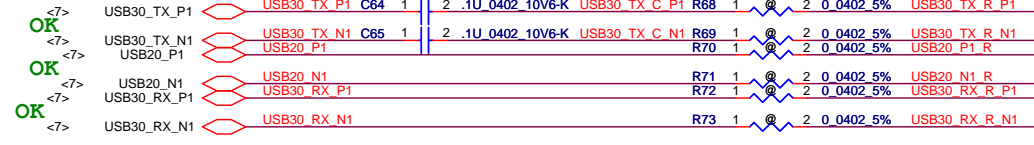


OK

OK

OK

For EMC

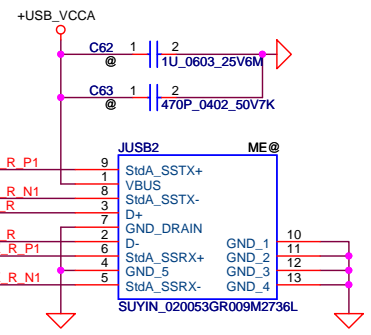


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OK <7>

OK <7>

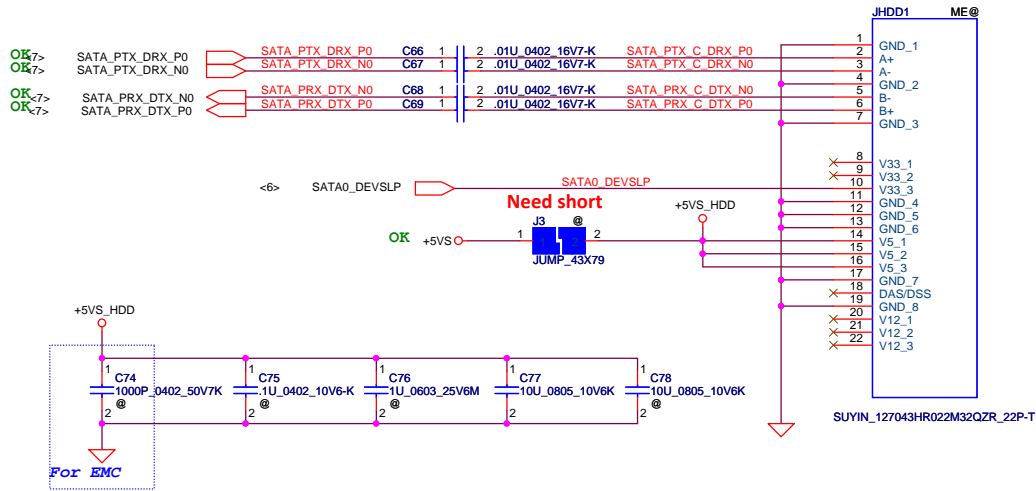
OK <7>



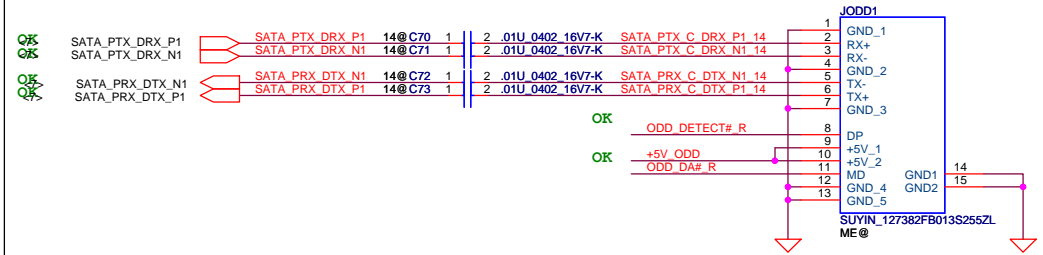
Security Classification	LC Future Center Secret Data		
Issued Date	2013/08/08	Deciphered Date	2013/08/05
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Title	USB2.0/USB3.0 PORT (LEFT)		
Size	Document Number	Rev	
Custom	NM-A281	0.4	
Date:	Thursday, February 20, 2014	Sheet	41 of 60

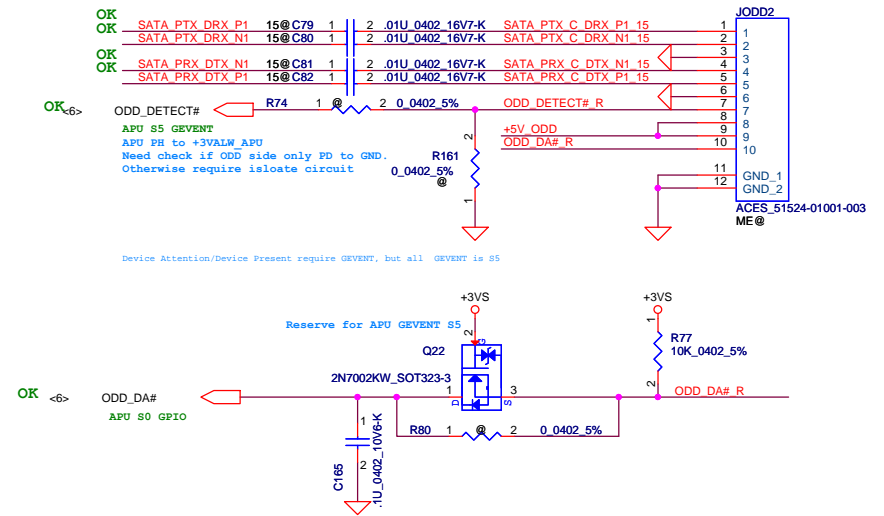
SATA HDD Conn.



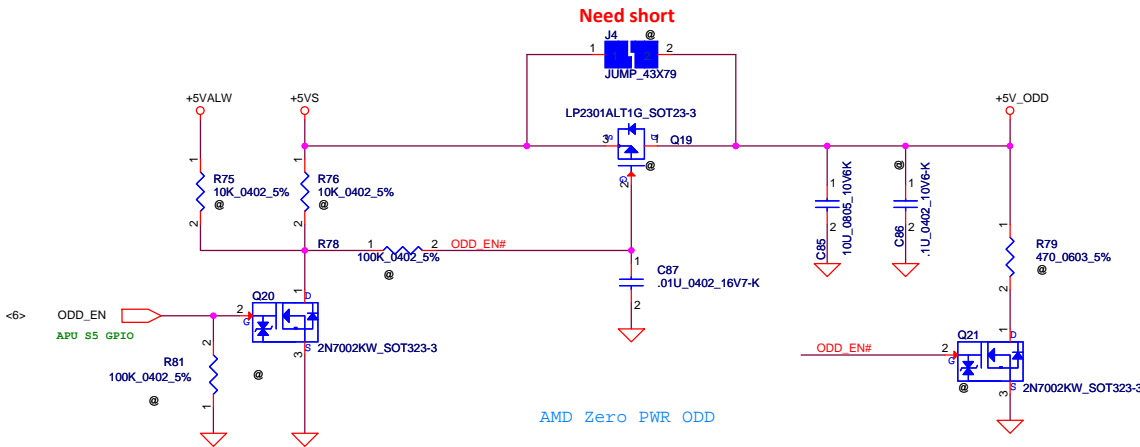
FOR 14" SATA ODD Conn.



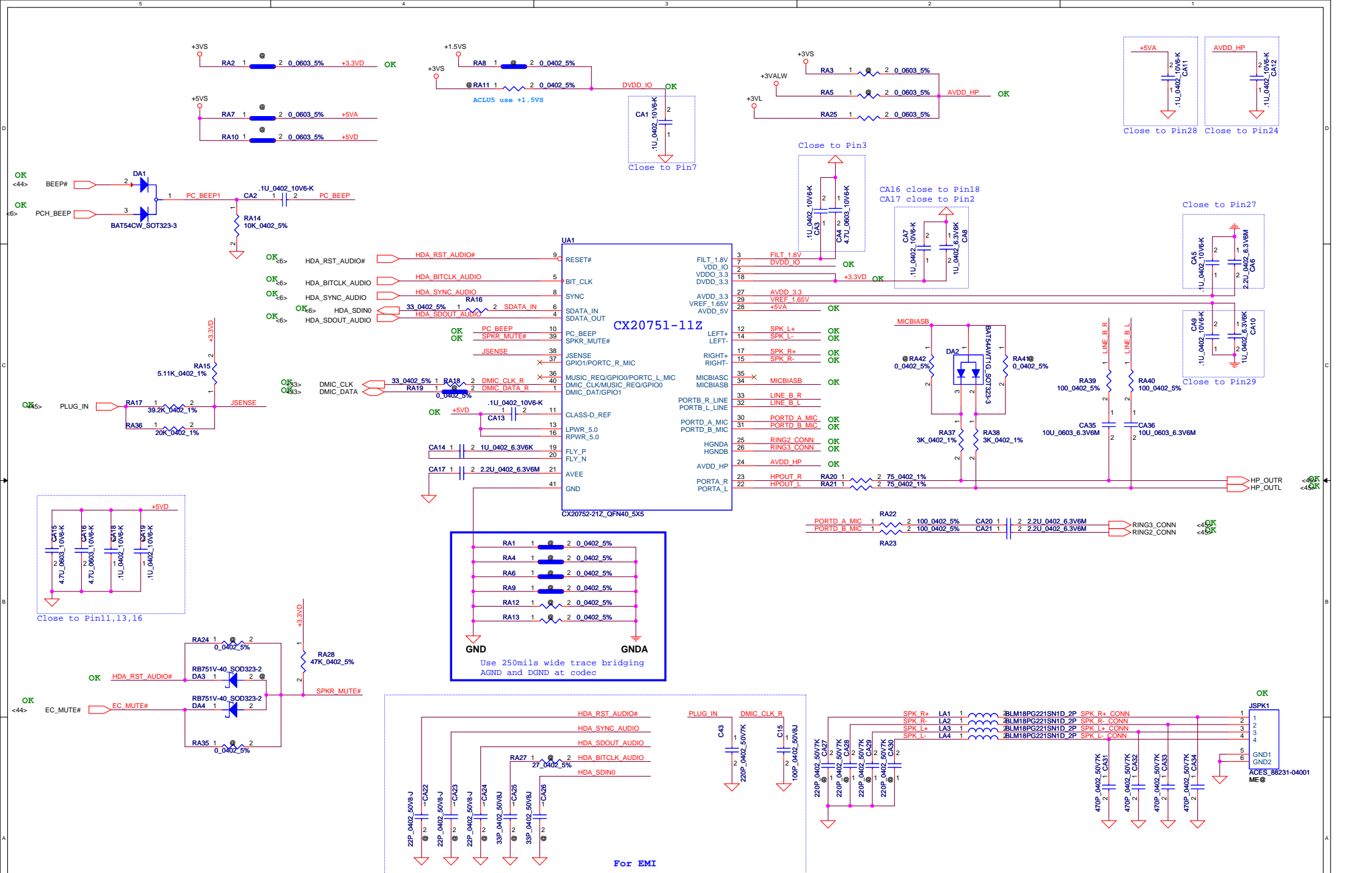
FOR 15" SATA ODD FFC Conn



+5VS to +5V_ODD OK

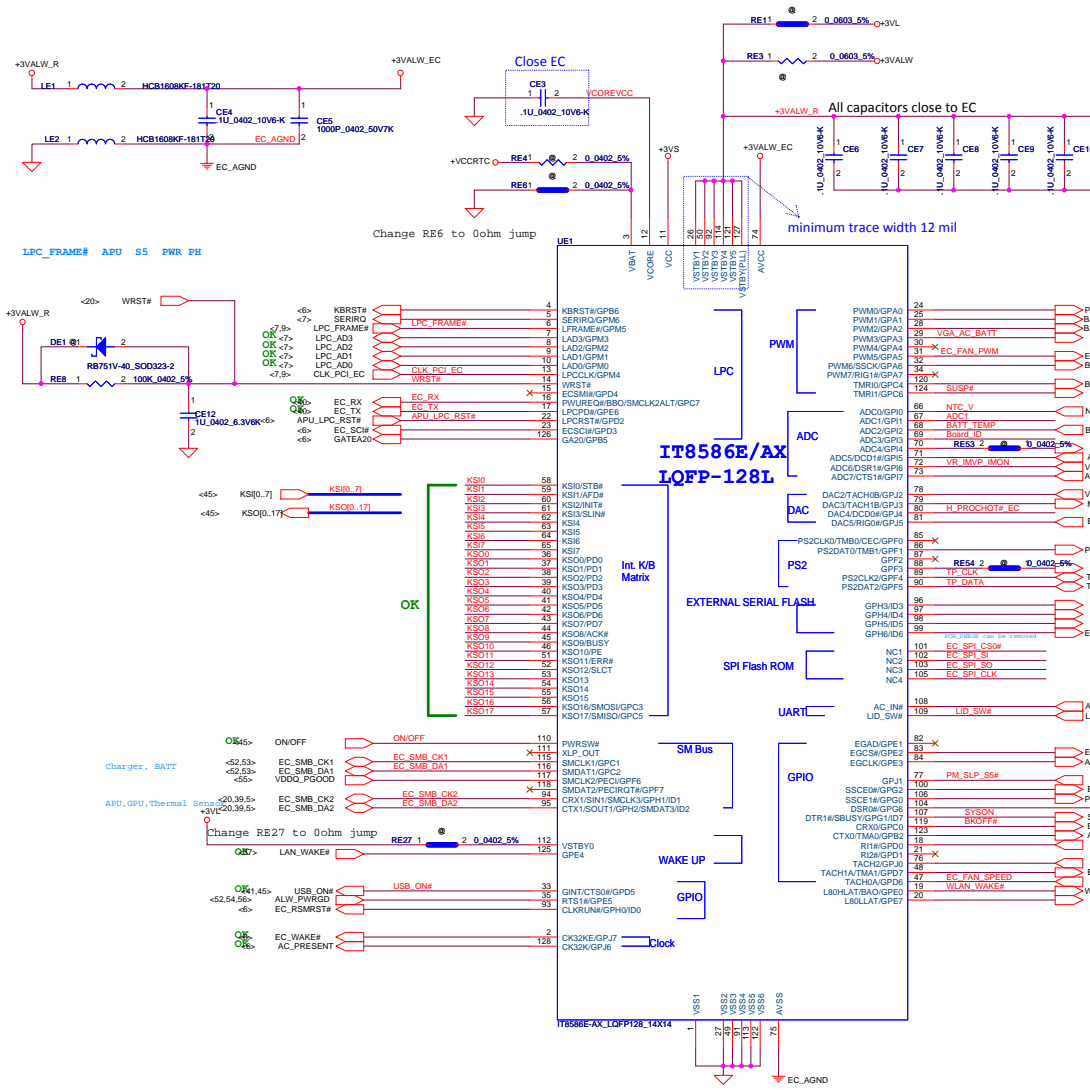


Security Classification				LC Future Center Secret Data				Title	
Issued Date				2013/08/08		Deciphered Date		2013/08/05	
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				Custom		NM-A281		0.4	
Date				Thursday, February 20, 2014		Sheet		42 of 60	



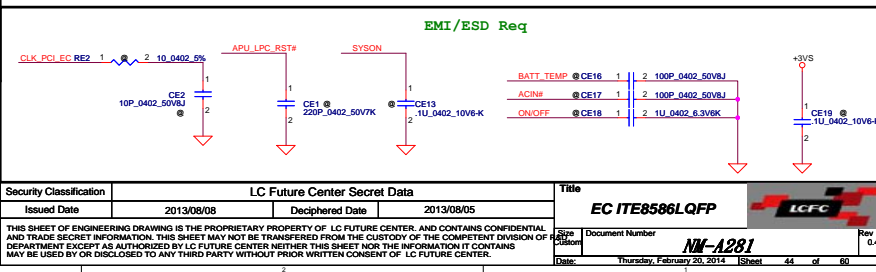
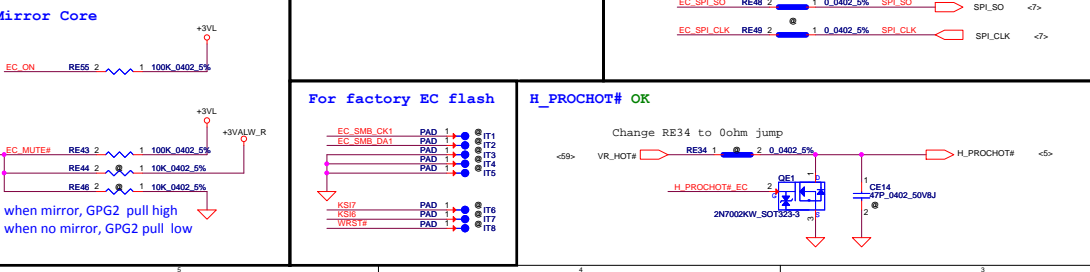
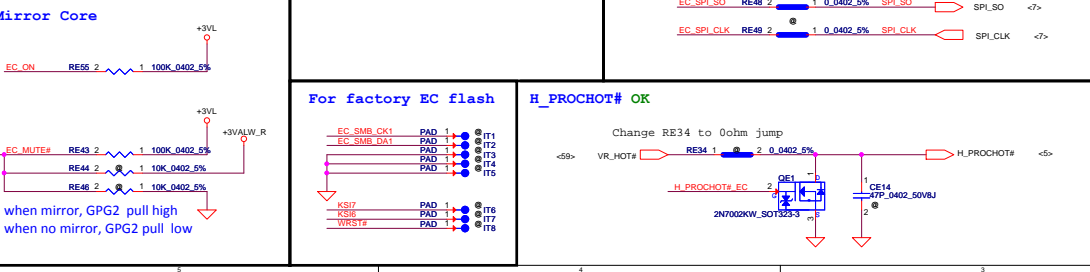
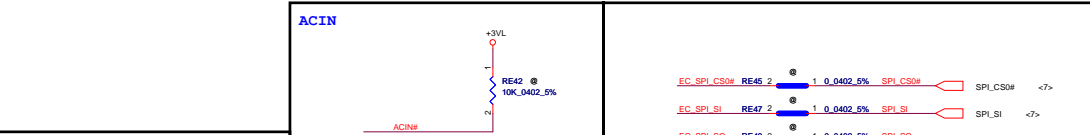
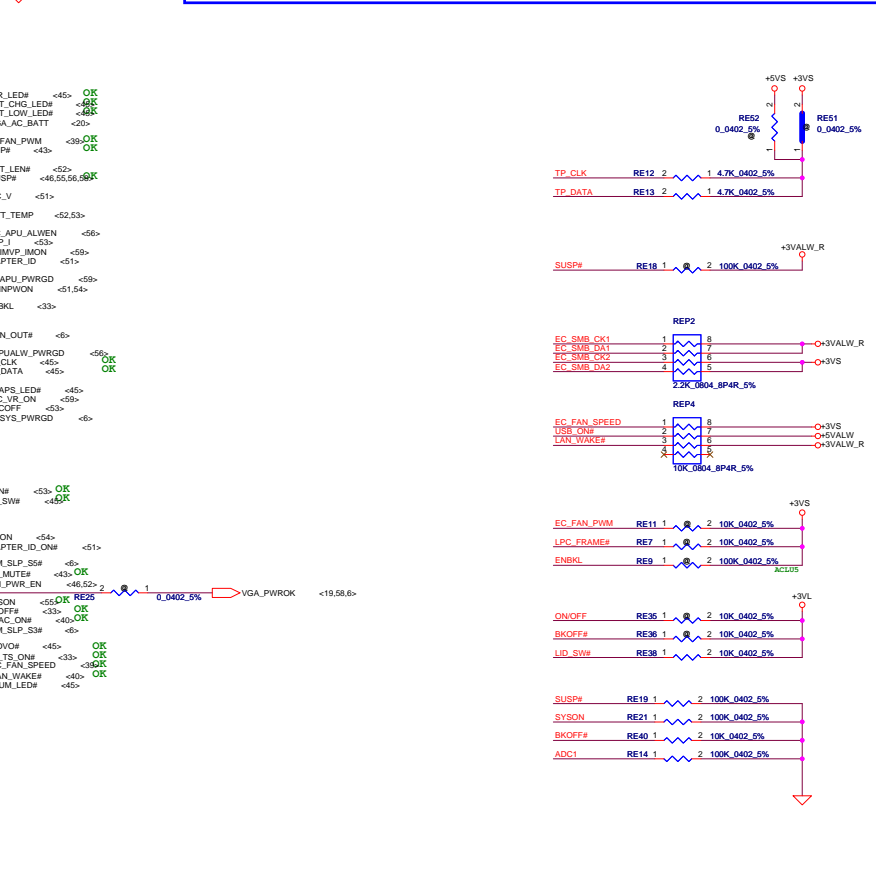
Issued Date	Deciphered Date	2013/08/05
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LC Future Center Secret Data	Title	Size	Document Number	Rev
2013/08/08	Codec_CX20752	Custom	NM-A281	0.4
			Date: Thursday, February 20, 2014	Sheet 43 of 60



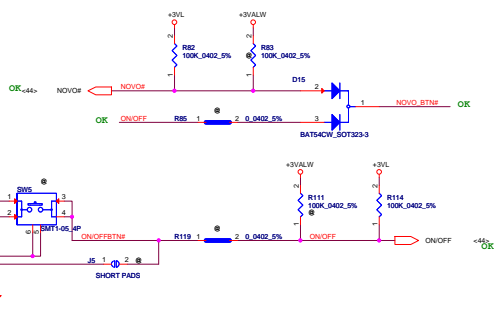
BORAD ID Config

Vcc	3.3V +/- 5%				
RE33	100K +/- 1%				
Board ID	RE34	V _{AD_BTD} min	V _{AD_BTD} typ	V _{AD_BTD} max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	
4	4.7K +/- 5%	0.141 V	0.148 V	0.155 V	
5	24K +/- 5%	0.612 V	0.638 V	0.664 V	



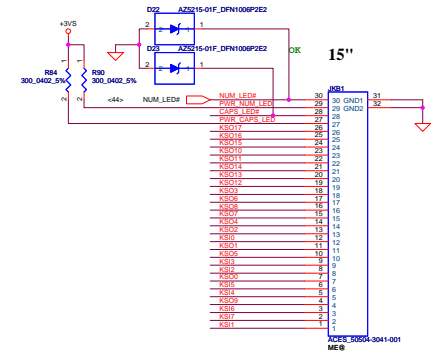
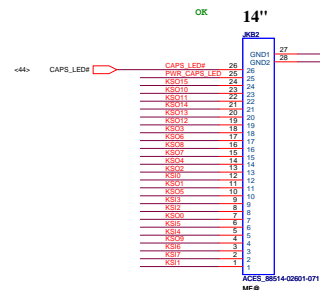
Security Classification	LC Future Center Secret Data	
Issued Date	2013/08/08	Deciphered Date
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Title	EC ITE8586LQFP	
Document Number	NW-A281	
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ON/OFF switch

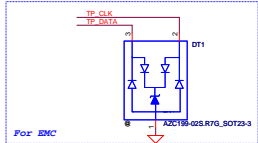
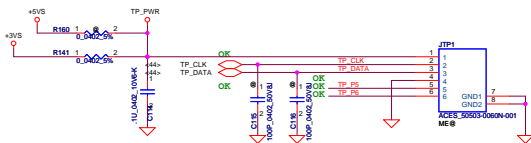


TP/B Connector

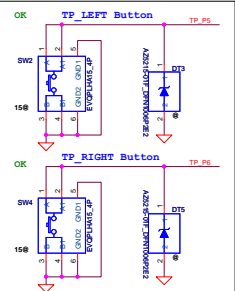
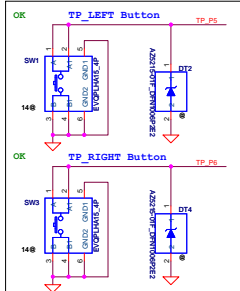
K/B Connector



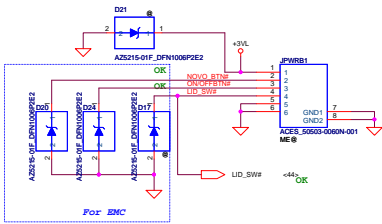
	14"	15"
KB_1	KS11_14	KS00_15
KB_2	KS17_14	KS12_15
KB_3	KS16_14	KS13_15
KB_4	KS09_14	KS05_15
KB_5	KS14_14	KS01_15
KB_6	KS18_14	KS10_15
KB_7	KS00_14	KS02_15
KB_8	KS12_14	KS04_15
KB_9	KS13_14	KS07_15
KB_10	KS05_14	KS08_15
KB_11	KS01_14	KS06_15
KB_12	KS10_14	KS03_15
KB_13	KS02_14	KS04_15
KB_14	KS04_14	KS01_15
KB_15	KS07_14	KS04_15
KB_16	KS08_14	KS01_15
KB_17	KS06_14	KS01_15
KB_18	KS03_14	KS05_15
KB_19	KS02_14	KS06_15
KB_20	KS03_14	KS07_15
KB_21	KS04_14	KB_LED_PWR
KB_22	KS01_14	KB_LED_PWM
KB_23	KS01_14	VDD_15
KB_24	KS01_14	NUM_LEDS_15



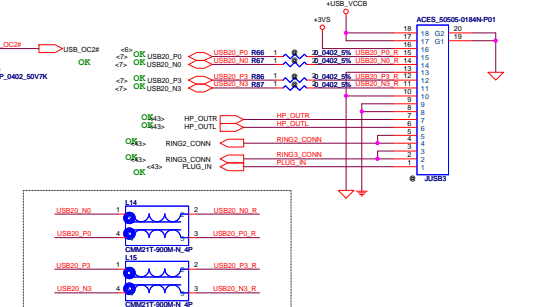
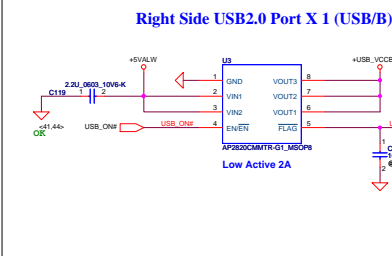
For 14"	For 15"
1 VDD	1 VDD
2 CLK	2 CLK
3 DAT	3 DAT
4 GND	4 GND
5 TP-L	5 TP-L
6 TP-R	6 TP-R



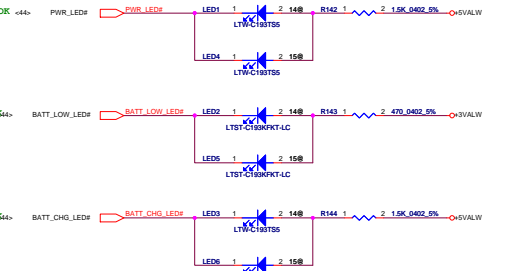
PWR/B Connector



USB I/O Connector

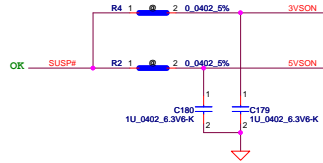


LED

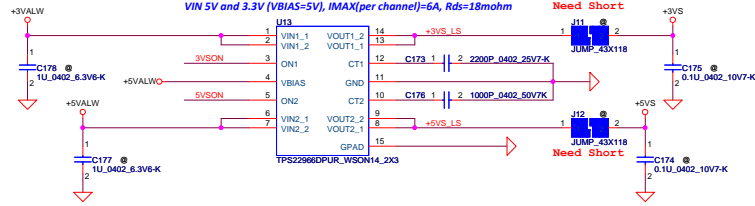


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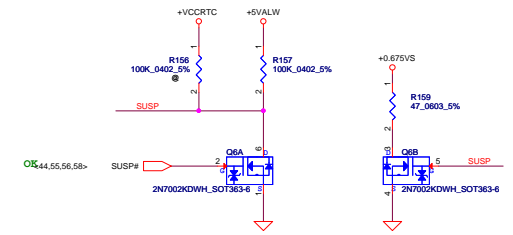
Load Switch
+5VALW To +5VS OK
+3VALW To +3VS



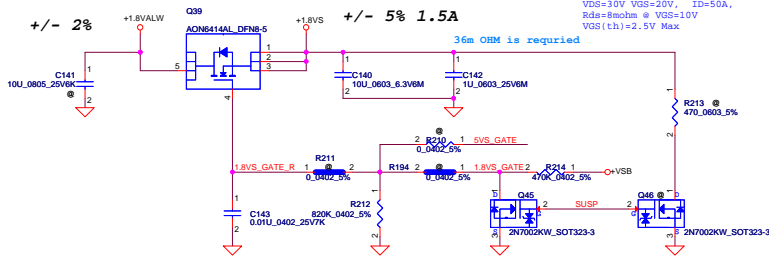
+5VS, C159 --> 1.5ms
+3VS, C160 --> 2.5ms



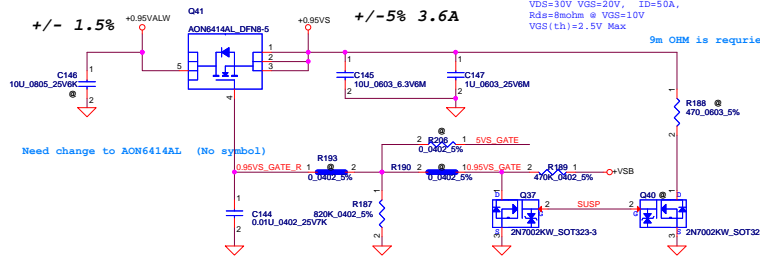
For DisCharge



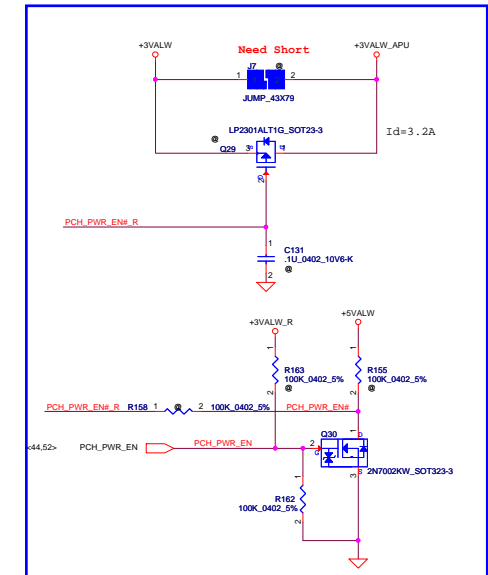
+1.8VALW to +1.8VS



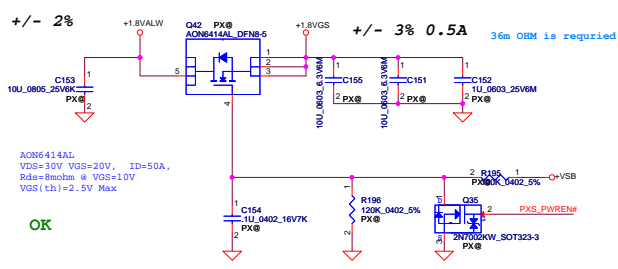
+0.95VALW to +0.95VS



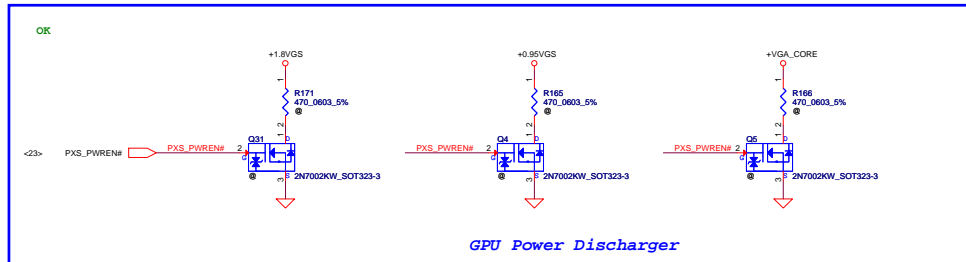
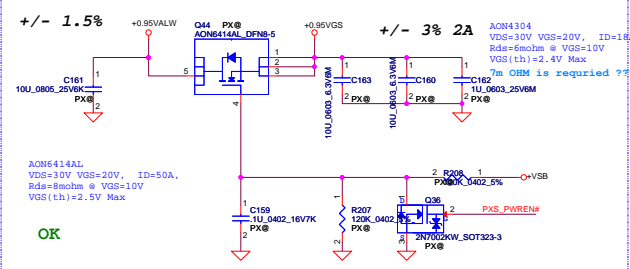
Need check all the EN pin and PWR Sequence.



+1.8VALW to +1.8VGS Reserve for GPU/APU share +1.8V



+0.95VALW to +0.95VGS Reserve for GPU/APU share +0.95V

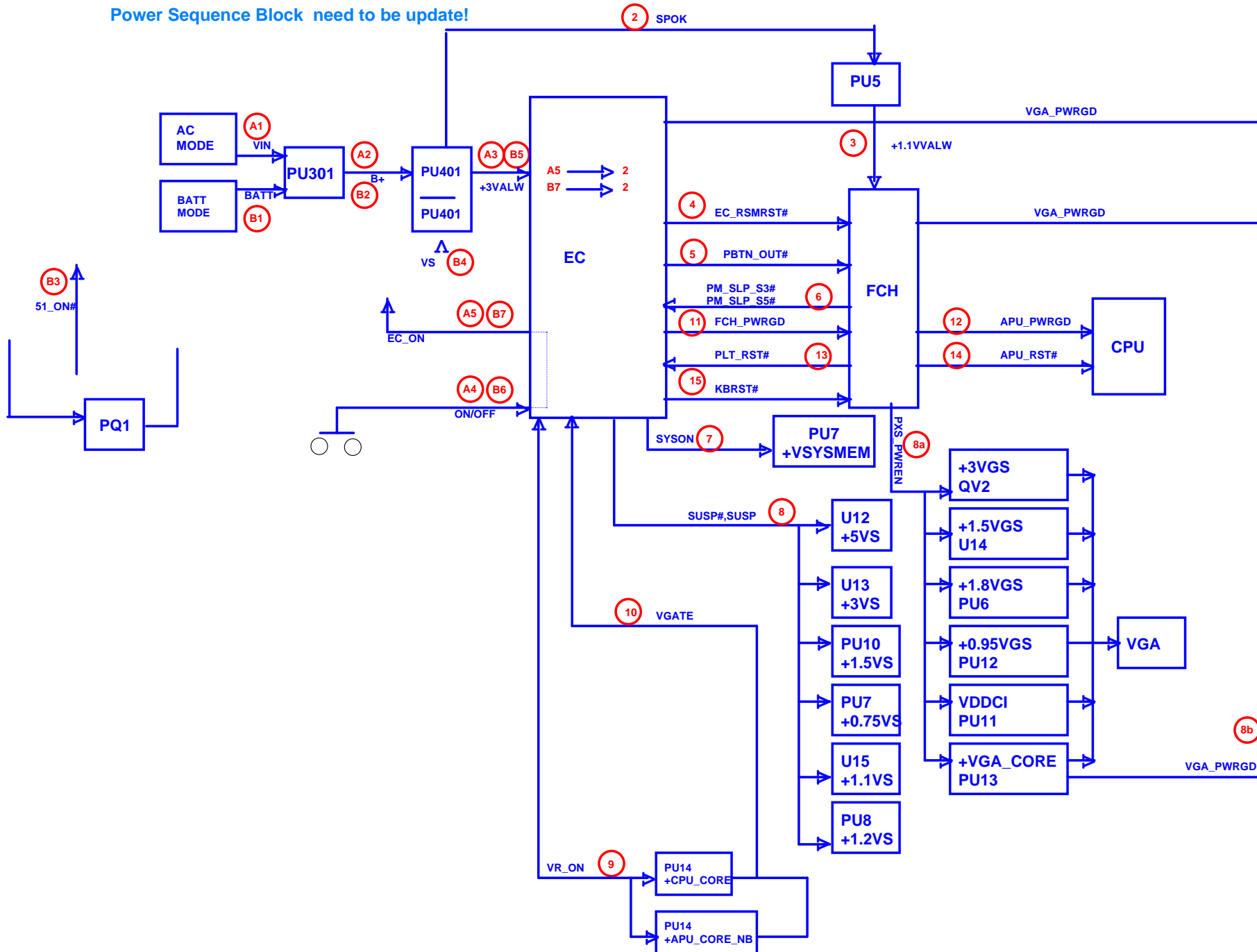


GPU Power Discharger

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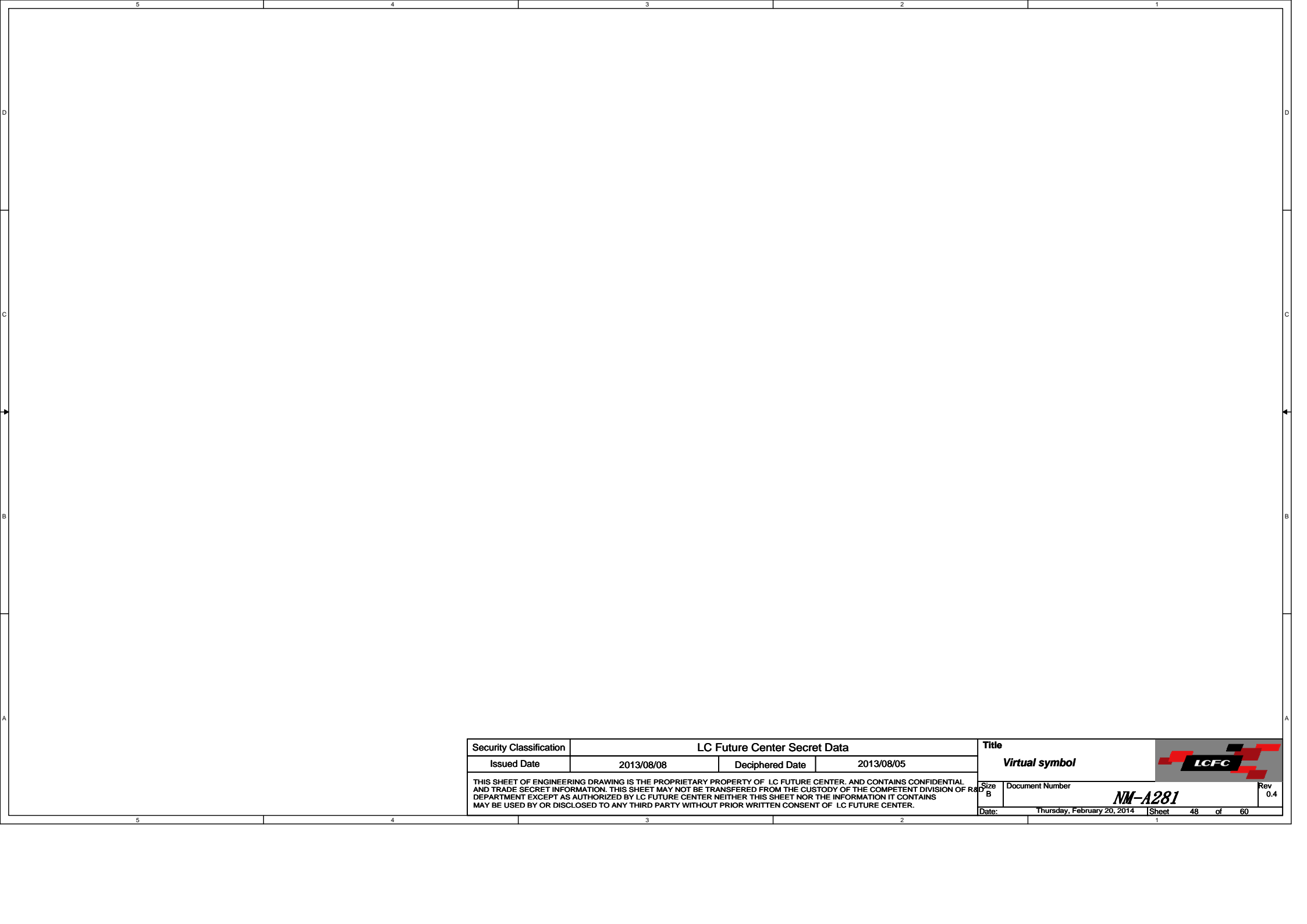
Power Sequence Block need to be update!



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5

4

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C


C

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B

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A

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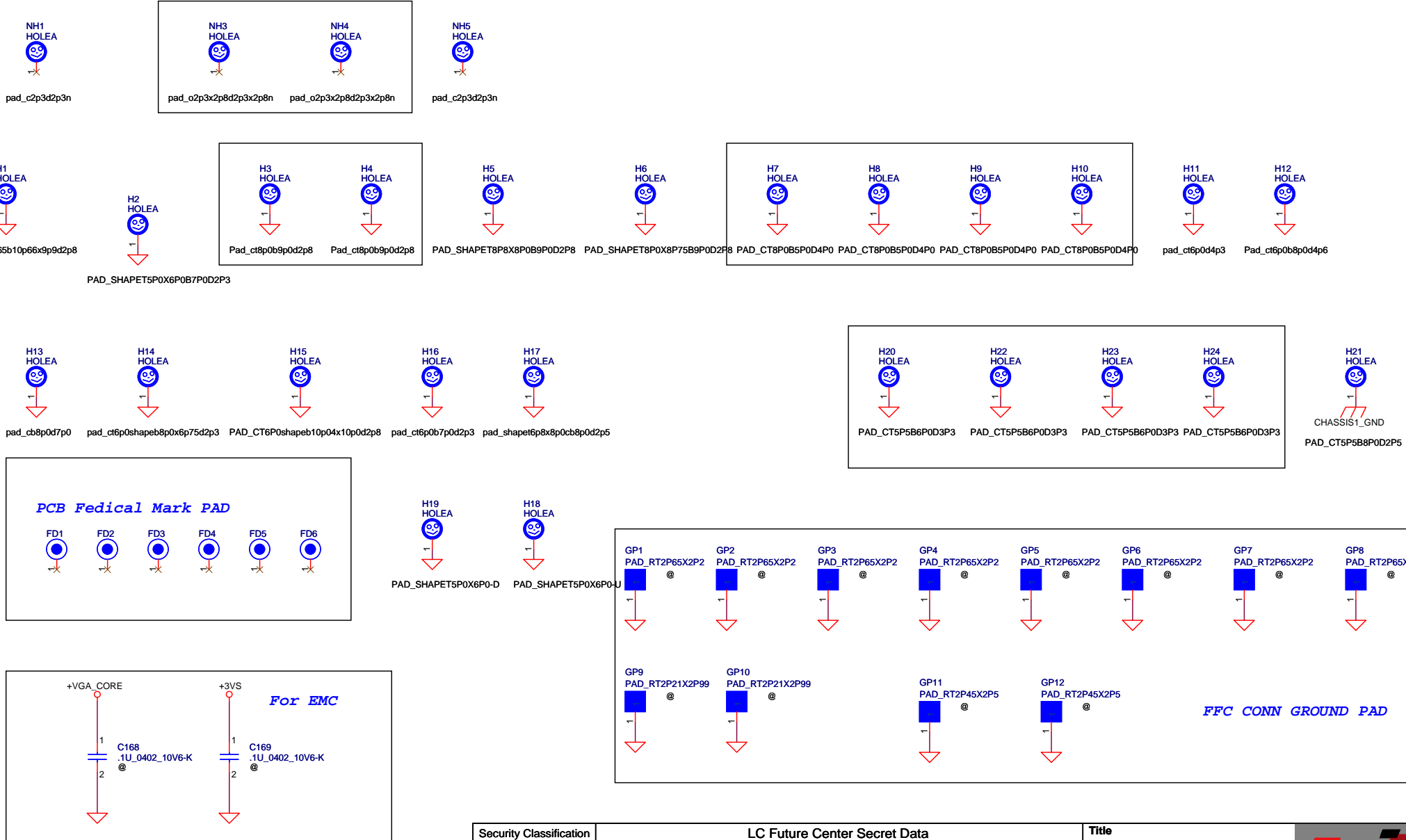
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4

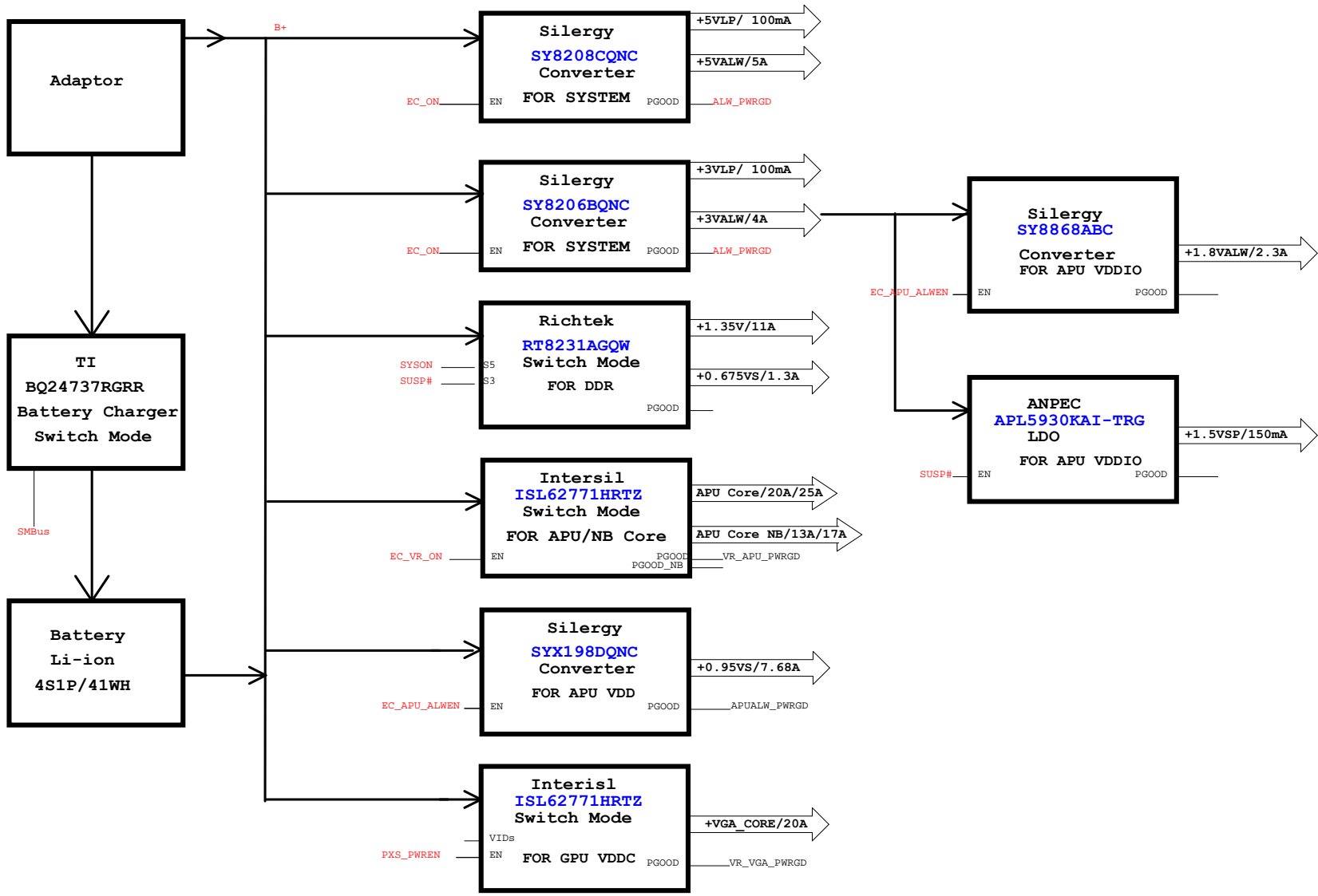
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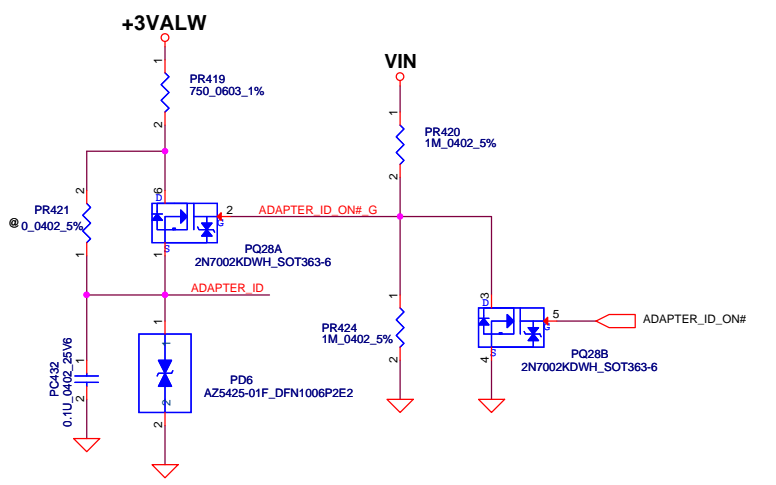
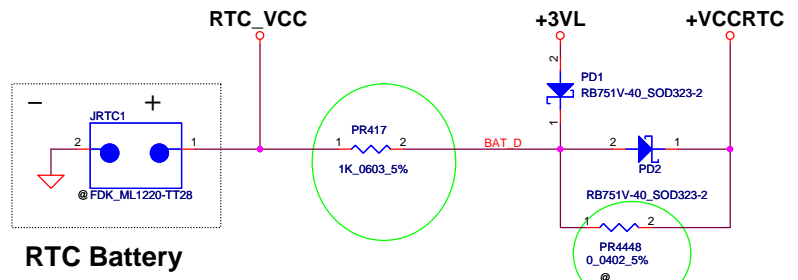
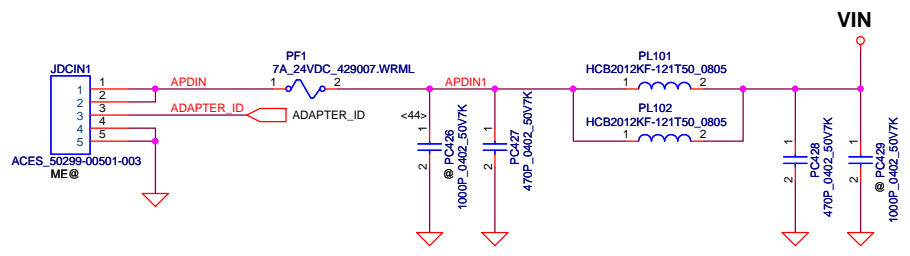
2

1

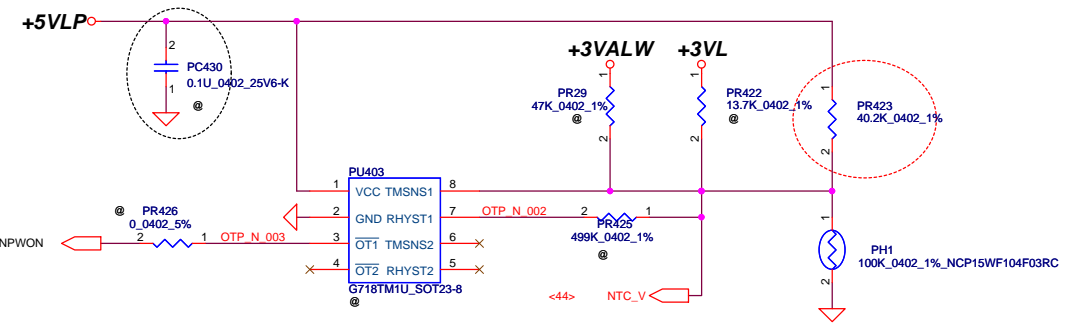


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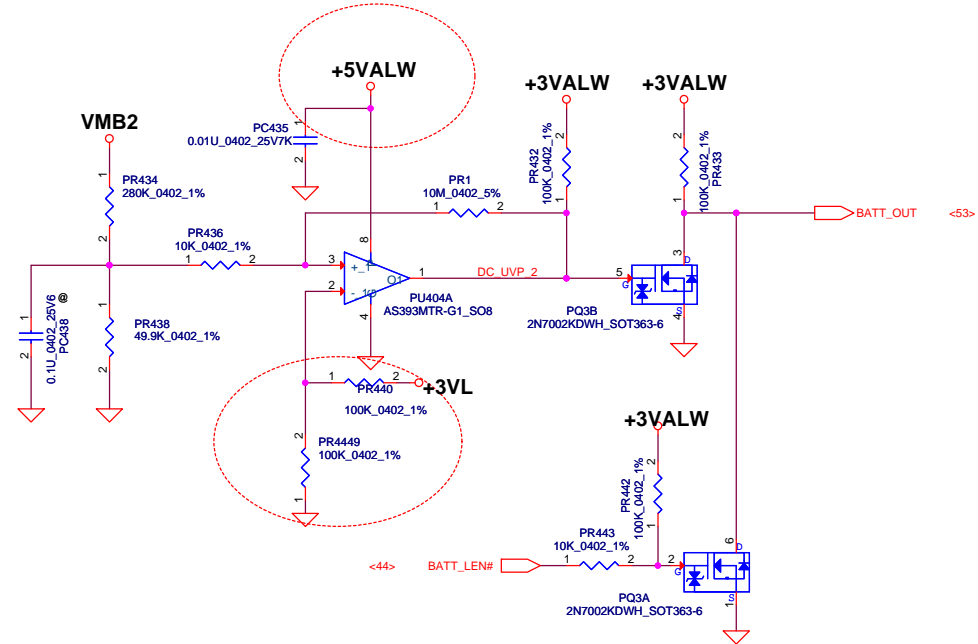
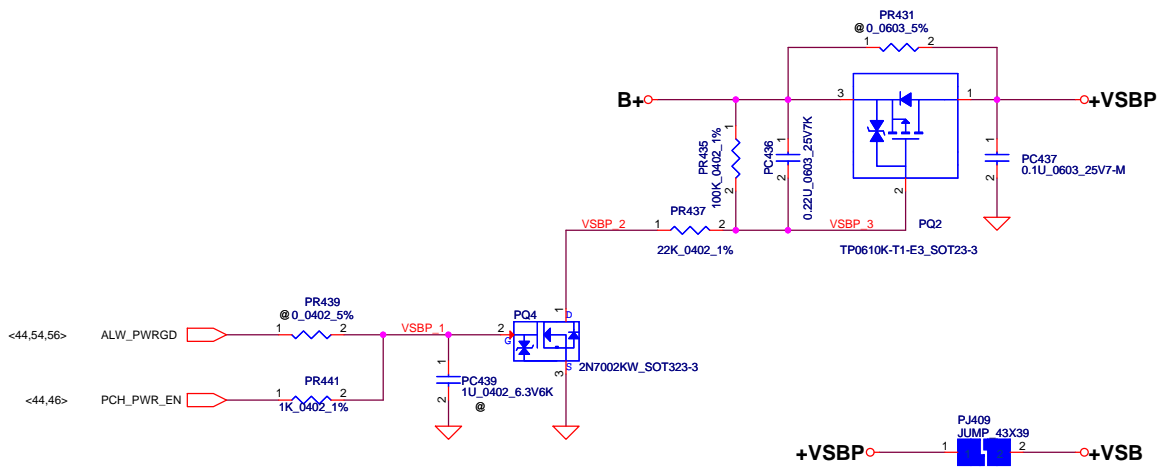
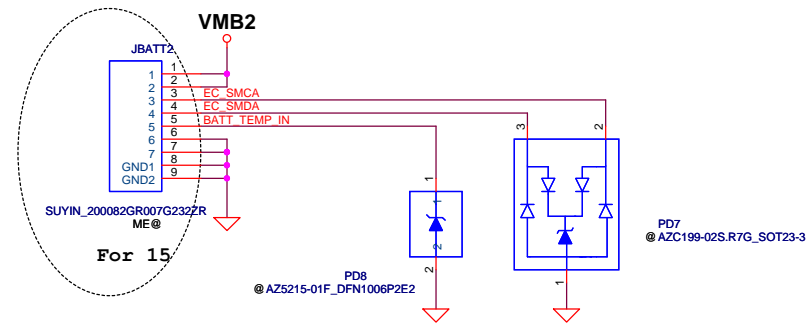
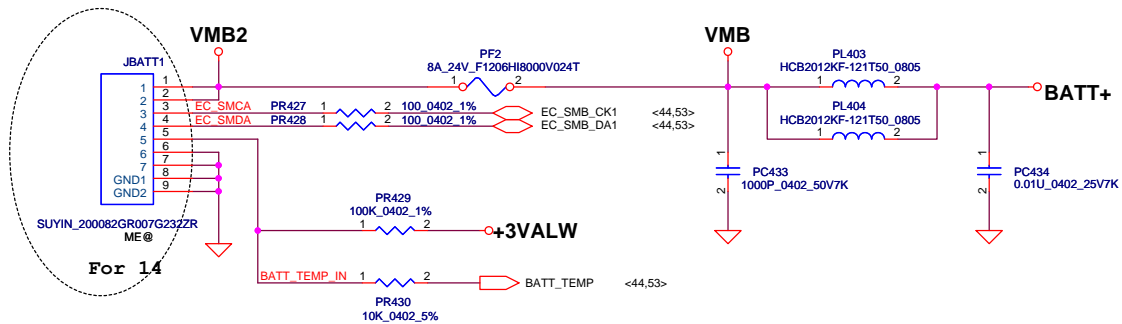
PH1 under CPU bottom side :
CPU thermal protection at 92+3 degree C
Recovery at 56 +3 degree C



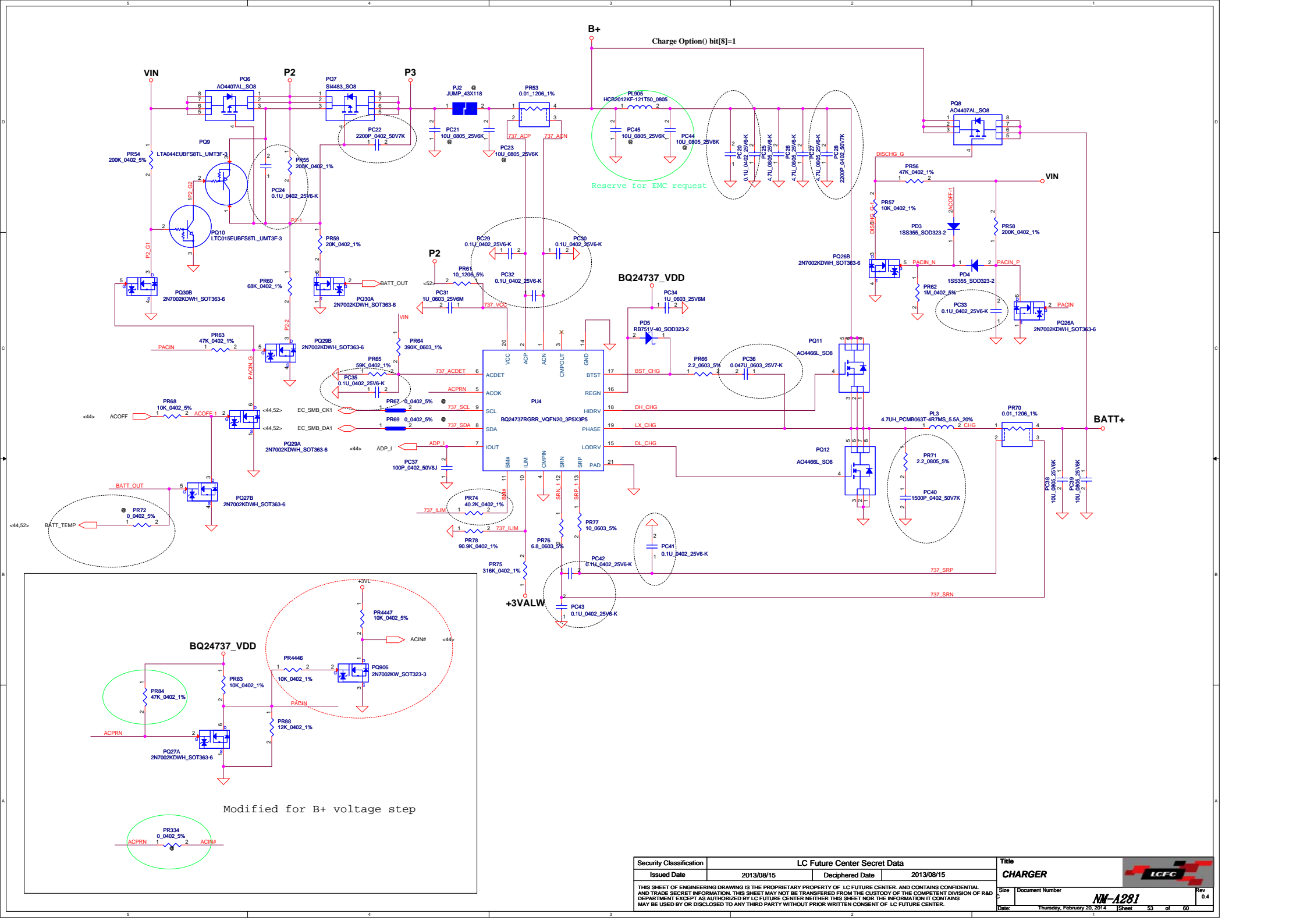
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Charge Option() bit[8]=1

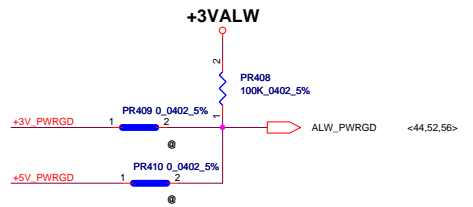
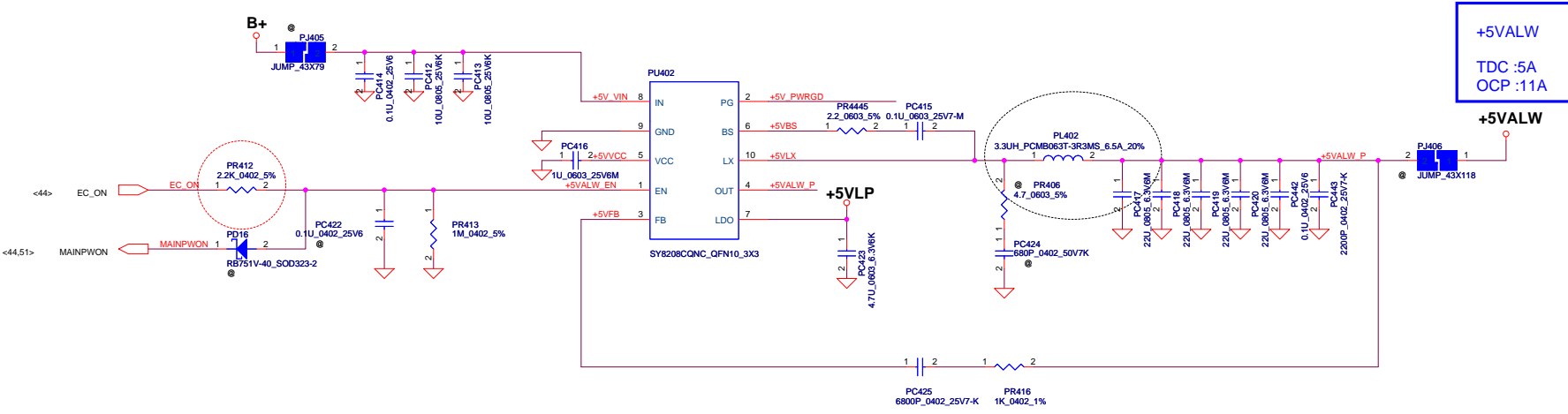
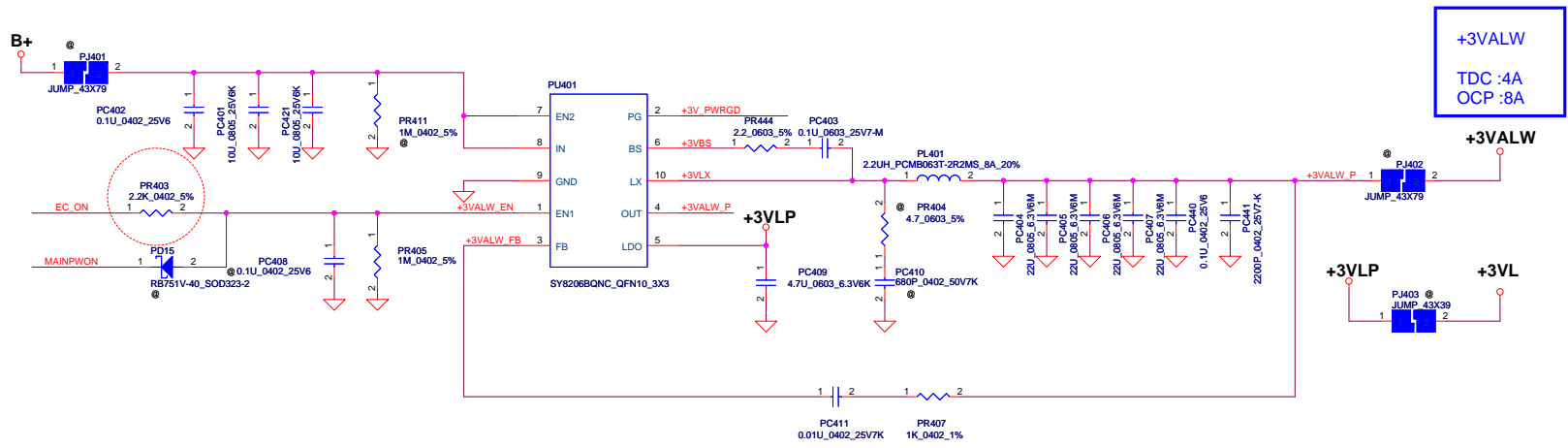
Reserve for EMC request

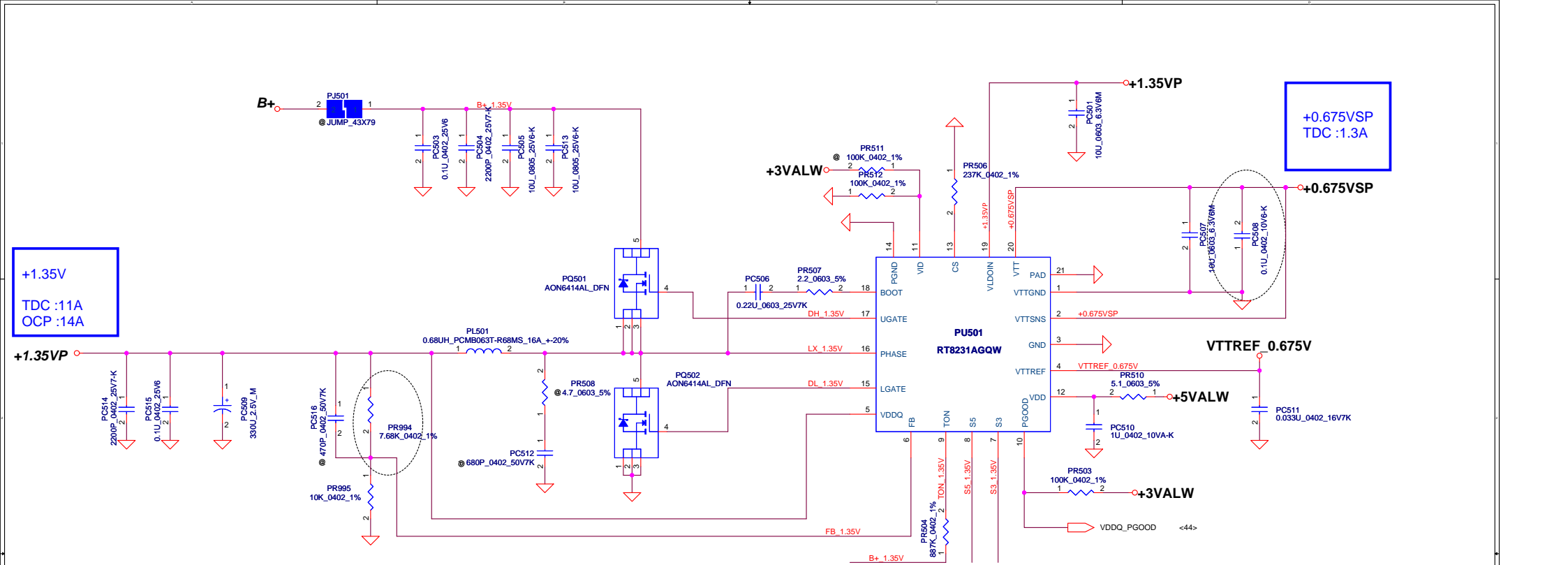
BQ24737_VDD

BQ24737_VDD

Modified for B+ voltage step

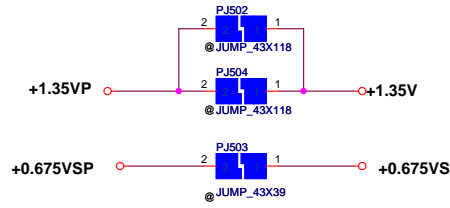
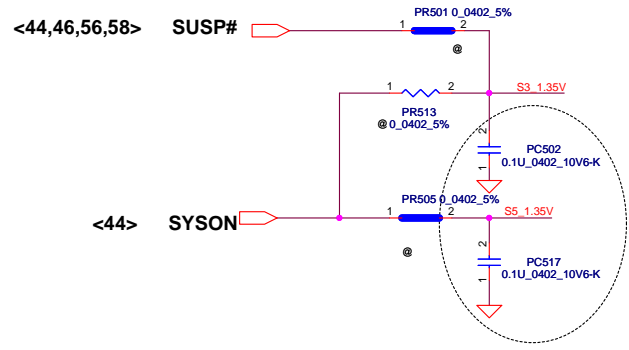
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+1.35V
TDC :11A
OCP :14A

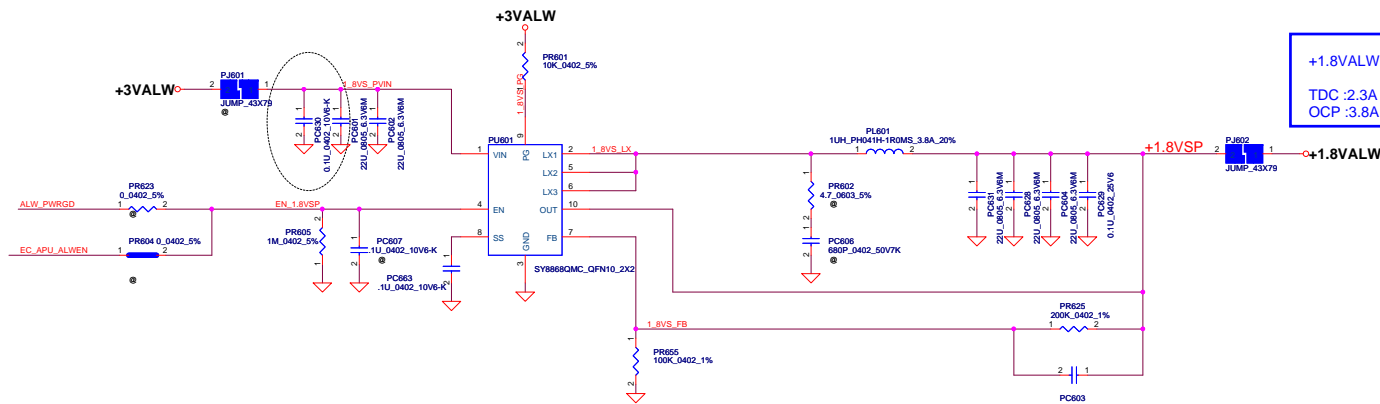
+0.675VSP
TDC :1.3A



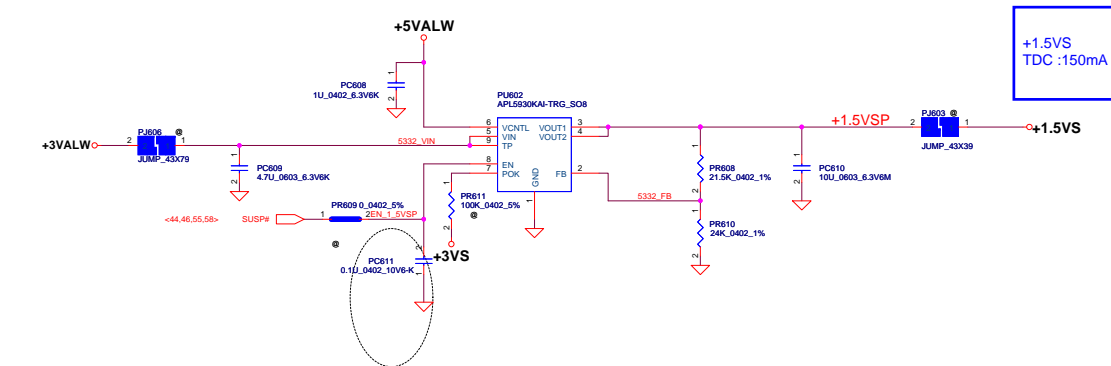
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Title	1.35VS/+0.675VS		
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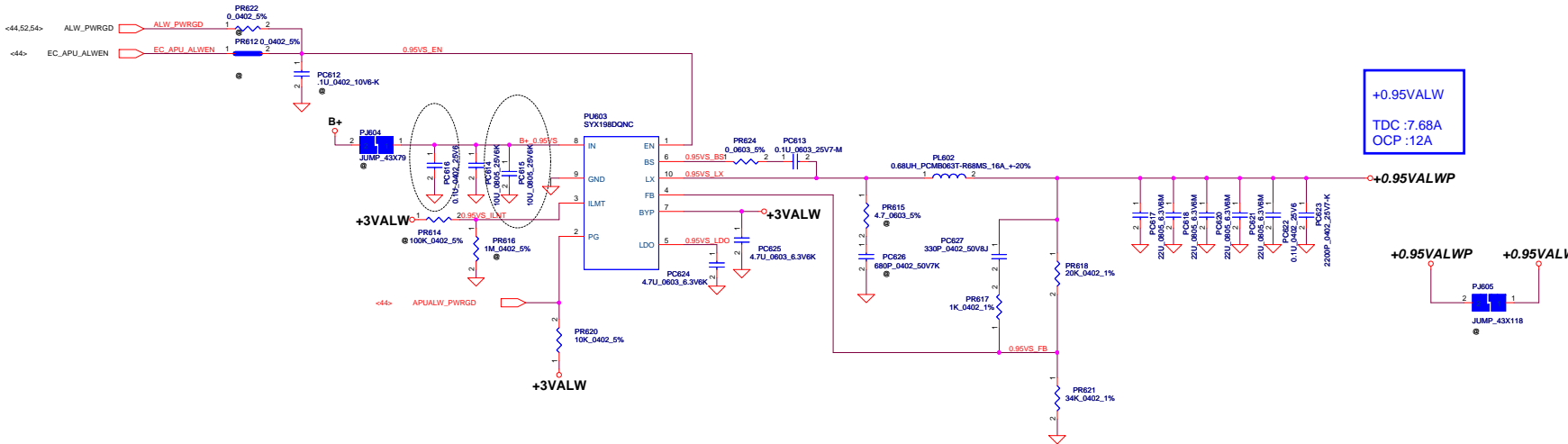




+1.8VALW
TDC :2.3A
OCP :3.8A

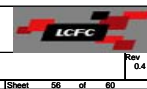


+1.5VS
TDC :150mA




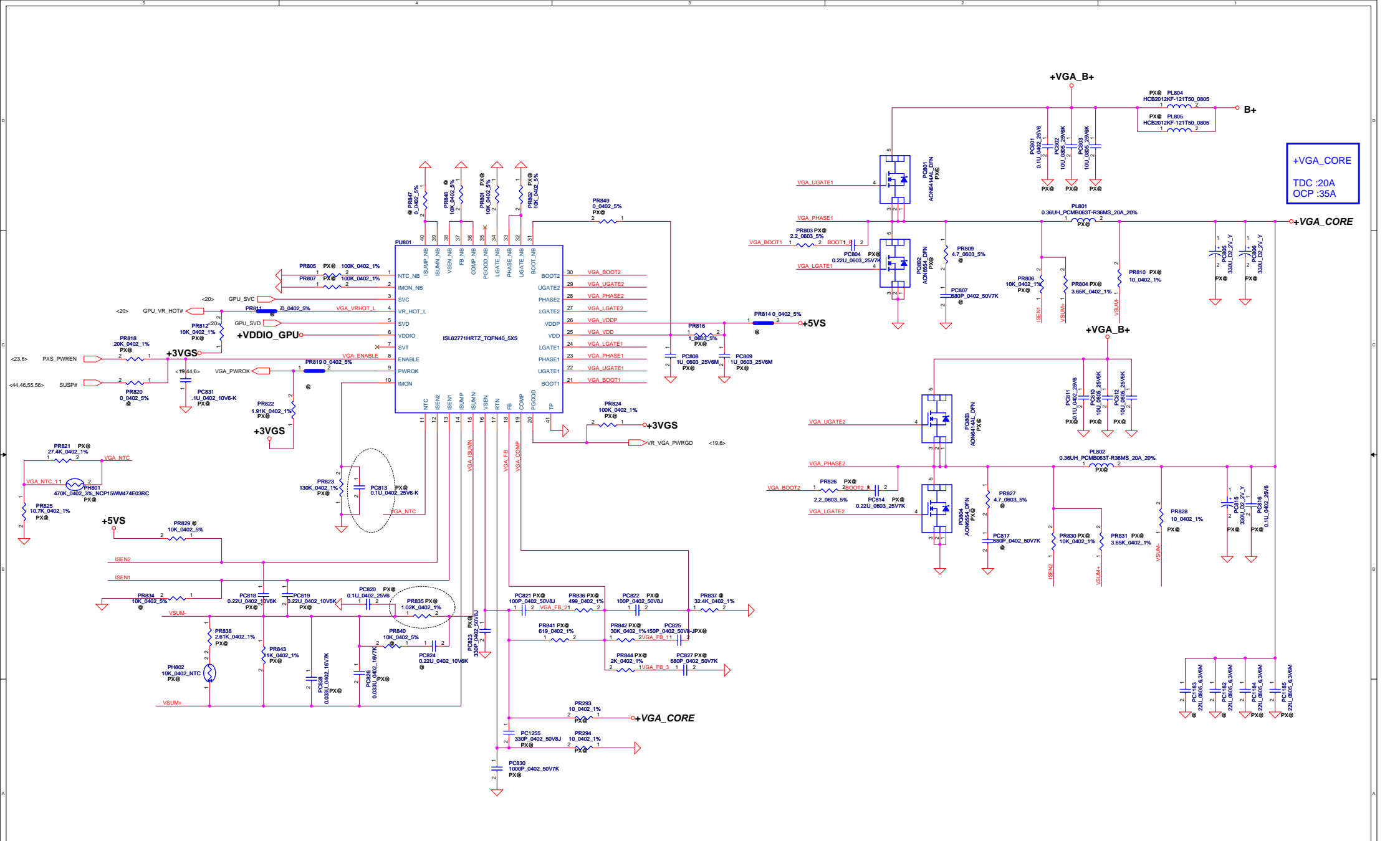
+0.95VALW
TDC :7.68A
OCP :12A

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			+1.35VS_VGA/+1.5VS
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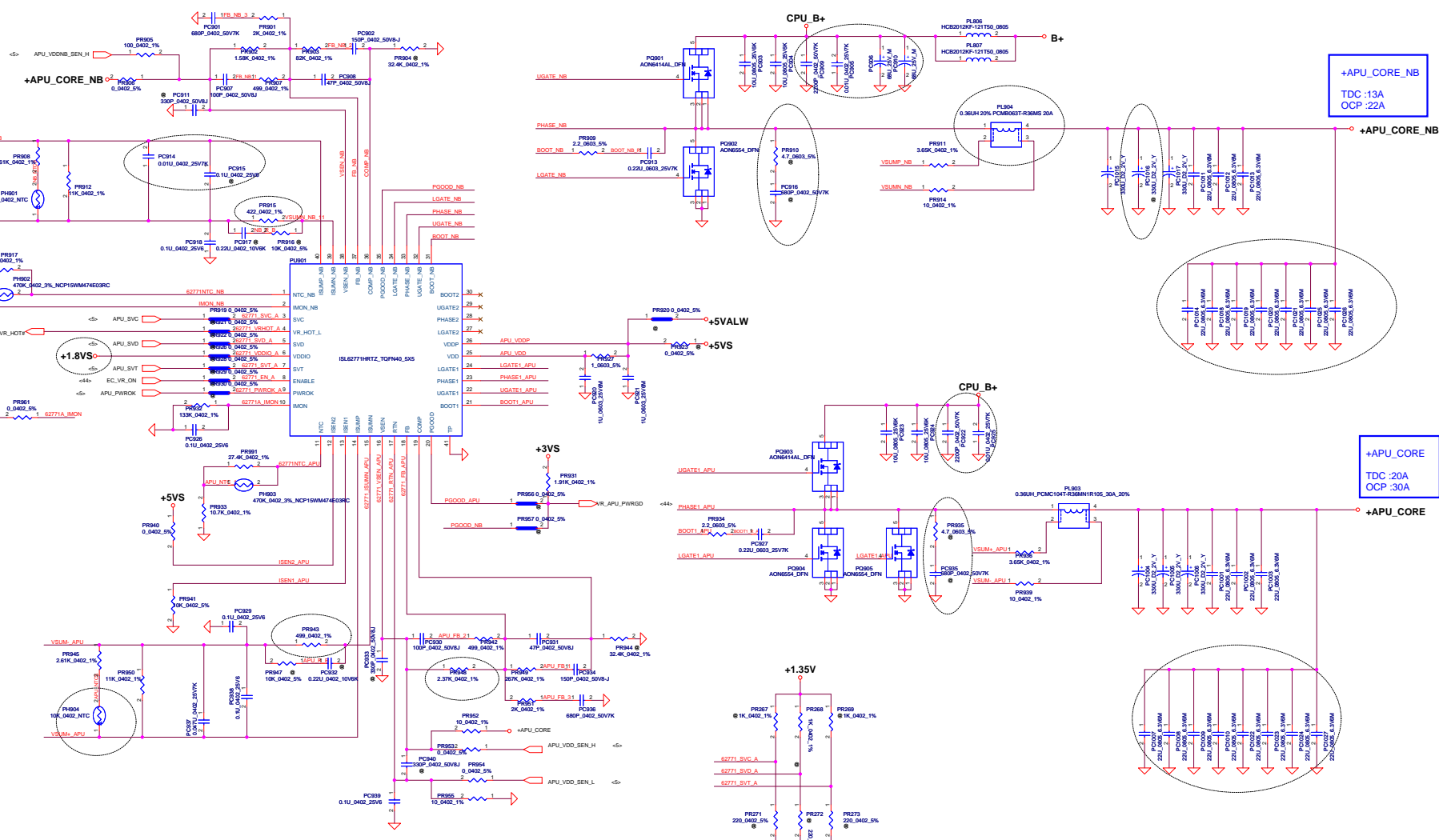


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+VGA_CORE
TDC :20A
OCP :35A

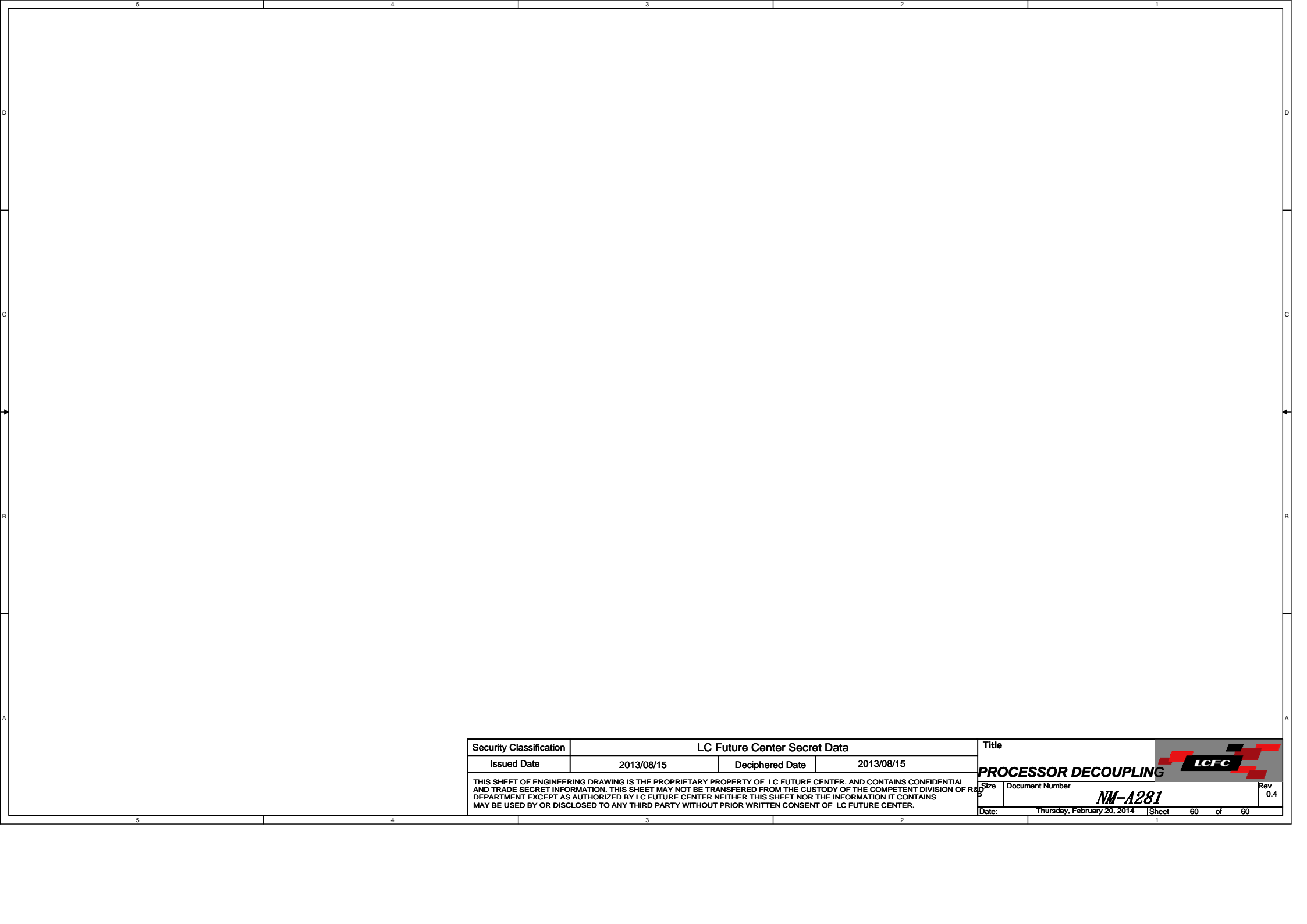
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PRE-PWROK METAL VID CODES

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V(Default)

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