

PG161-A00

TU106 6GB GDDR6, 192b, X16 DVI-D/DP + DP + HDMI

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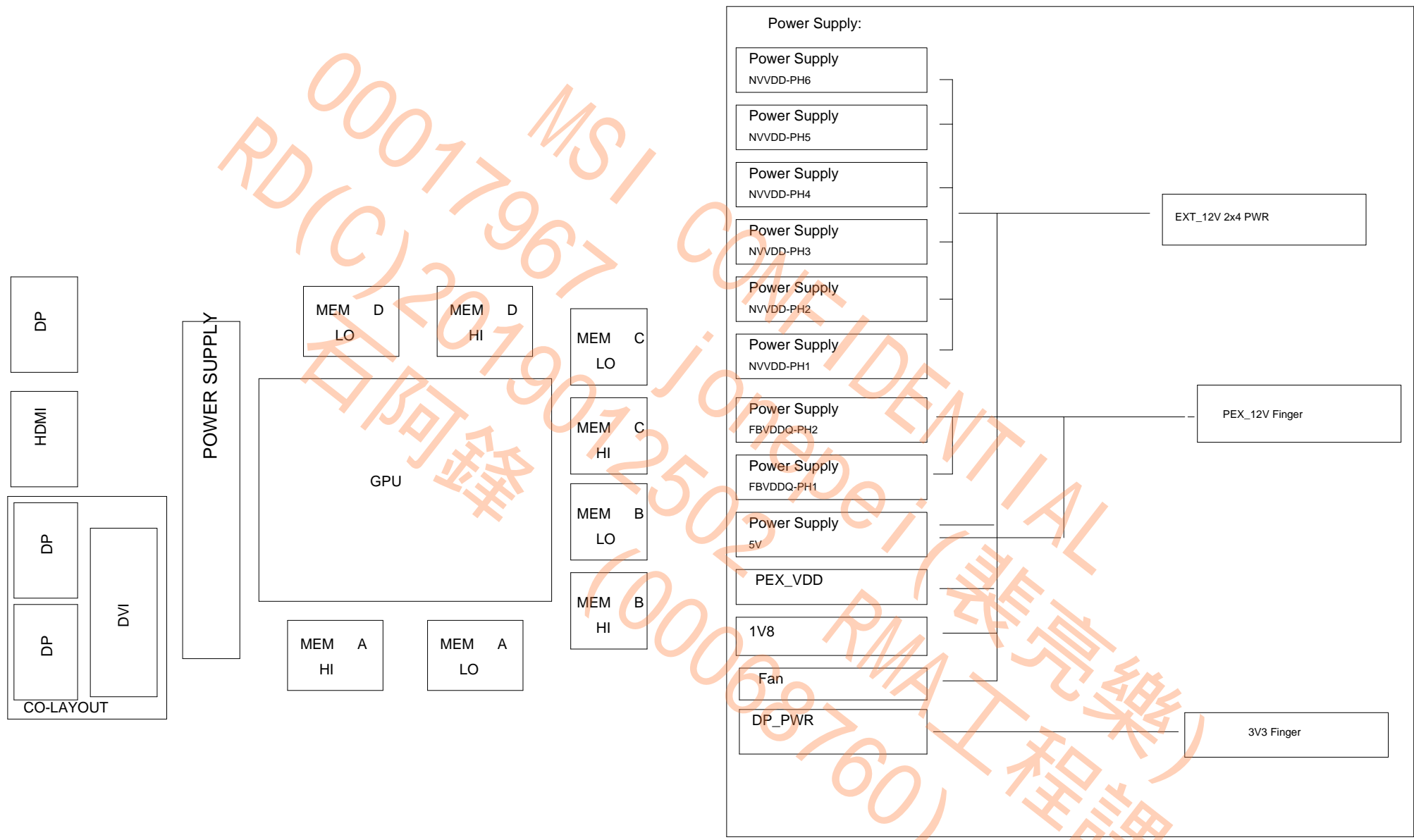
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- V375-20
 1. 移除 CO-LAY
 2. Core Power: uP9512SQKI (QFN 4x4) + (NCP302045 x 4)
 Memory Power: I32-S725602-N03 + (UBIQ 3103+3107*2)
 3. P.34 add R779
 4. P.30 & 44 移除PS_FBVDQ_BUFF換頁符號
 換FBVDQ controller · 換成1PHASE 上1下2
 5. P.52 add HDMI & DVI 螺絲
 6. IO 換常用料 · footprint 不變

000719MSI
RD(C)2018
石阿對線(00068760)
jonepei (裝亮樂)
RMA工程師

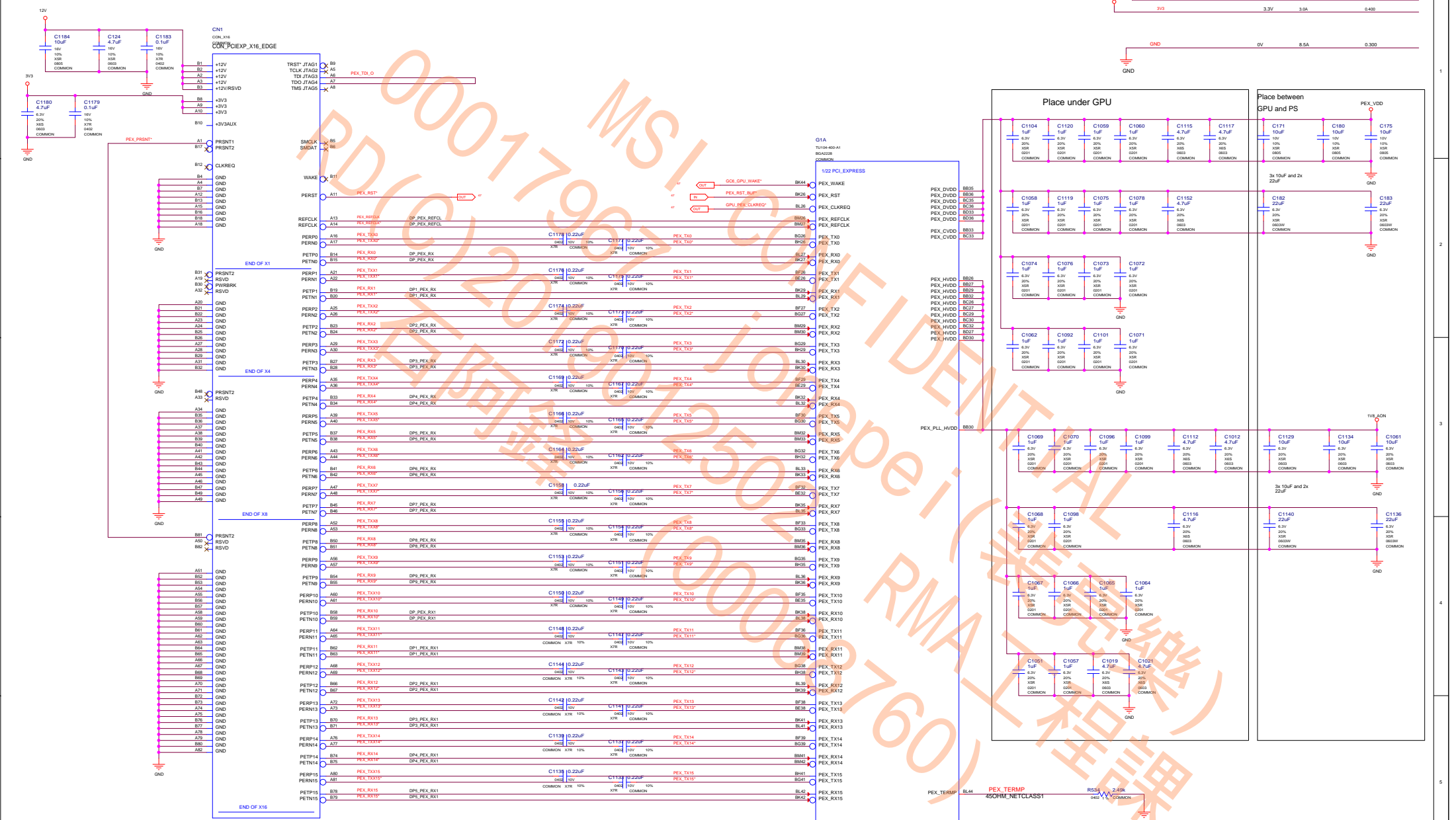
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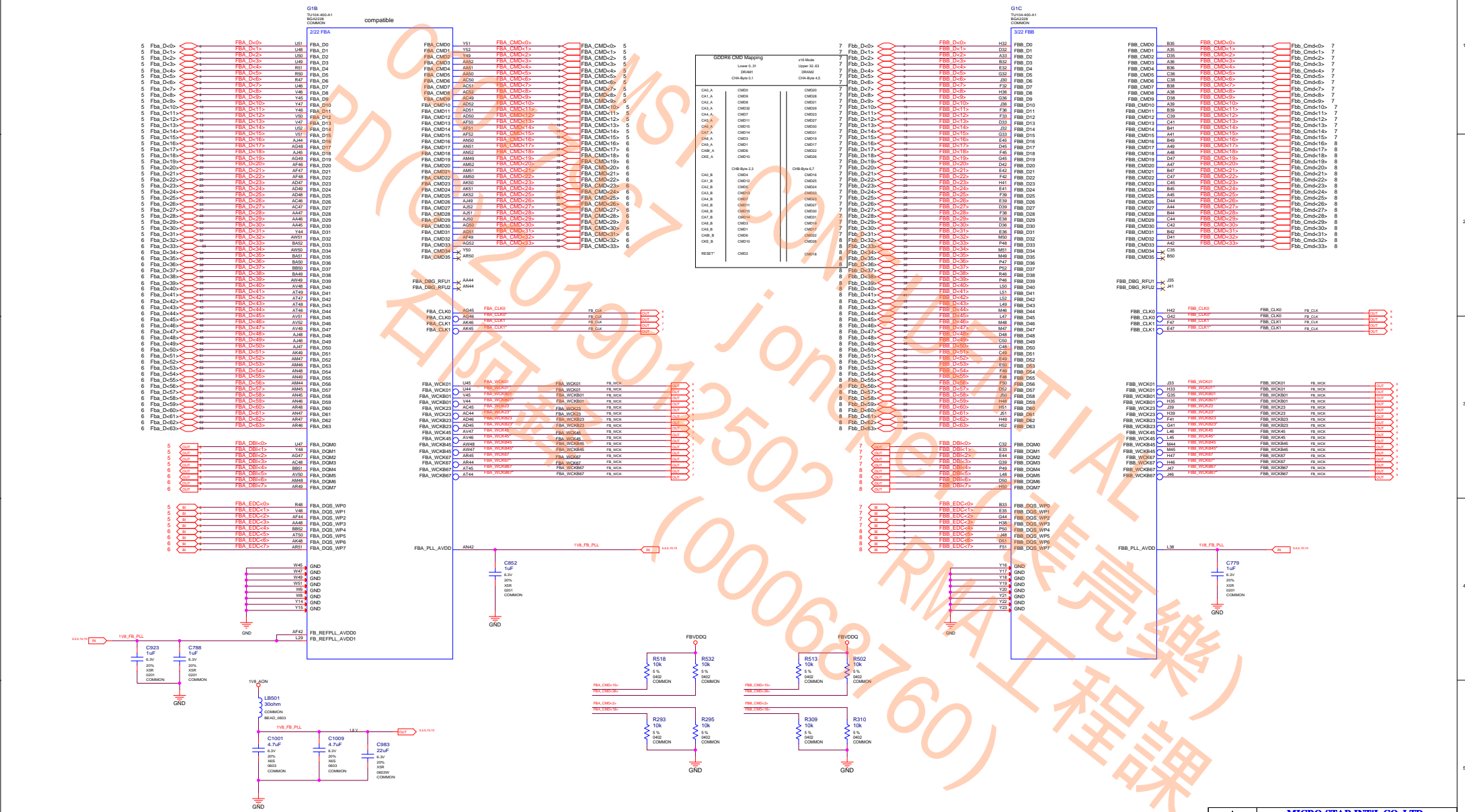
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NO PEX GEN4 SUPPORT DELETE RC TERMINATIONS

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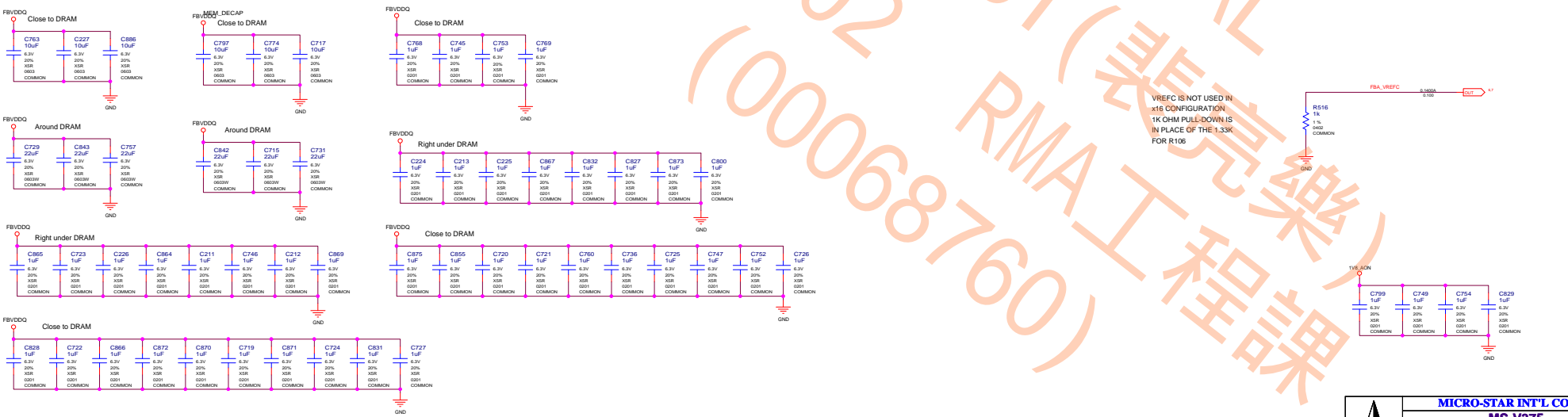
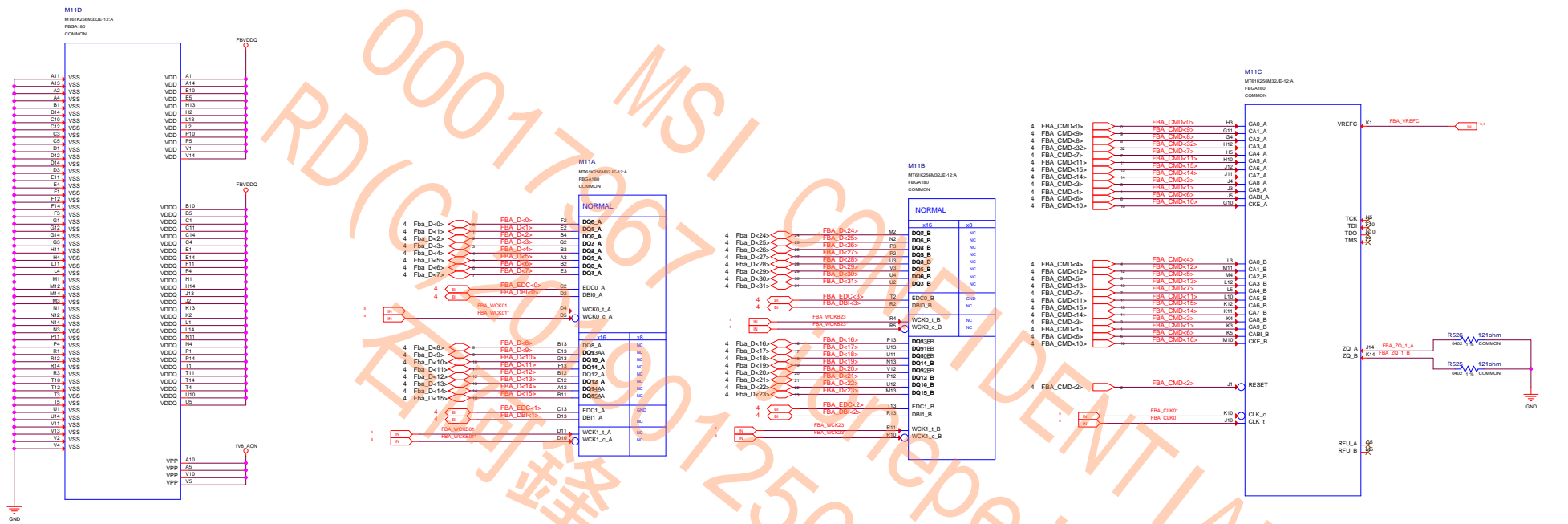
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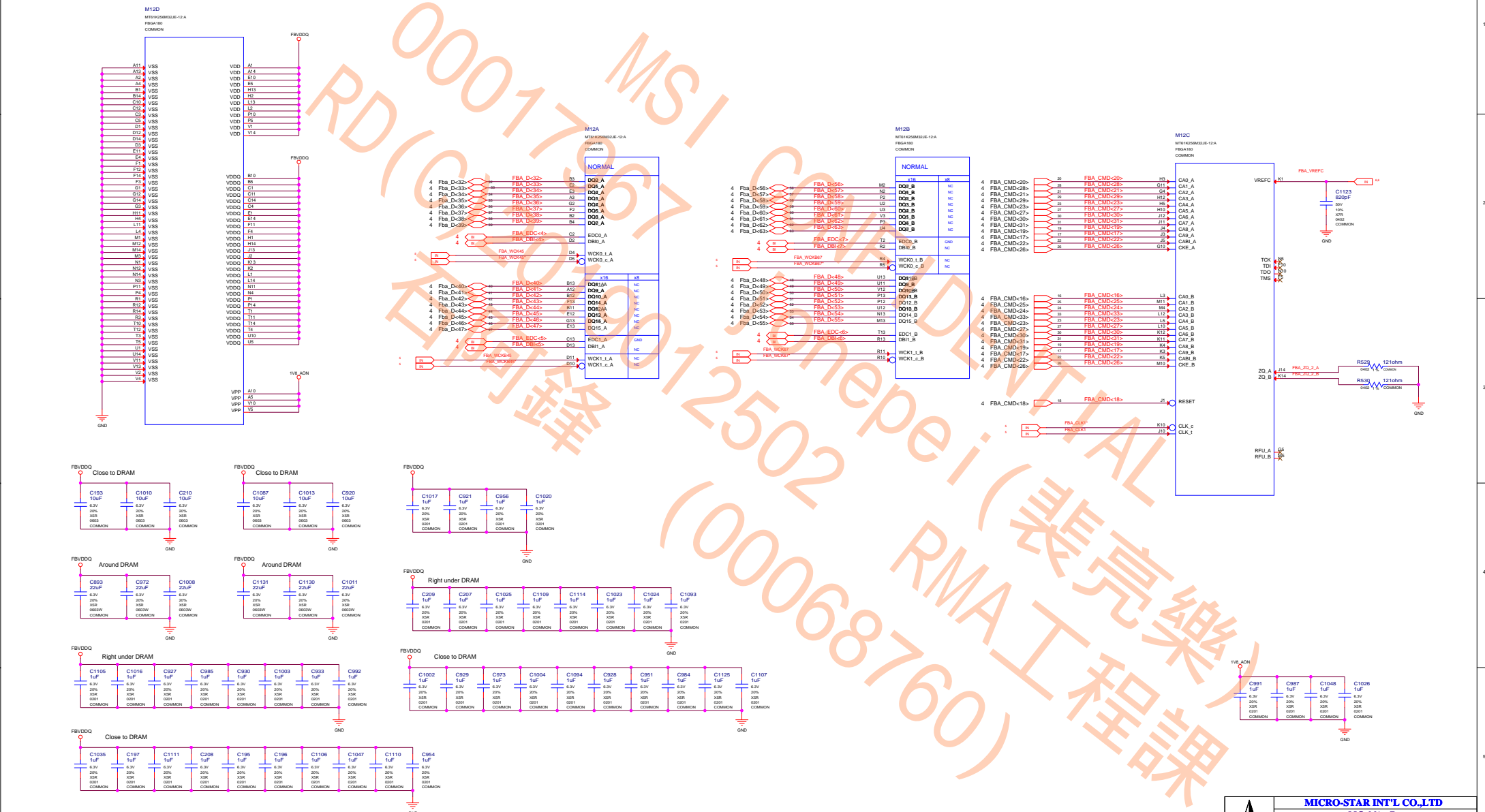
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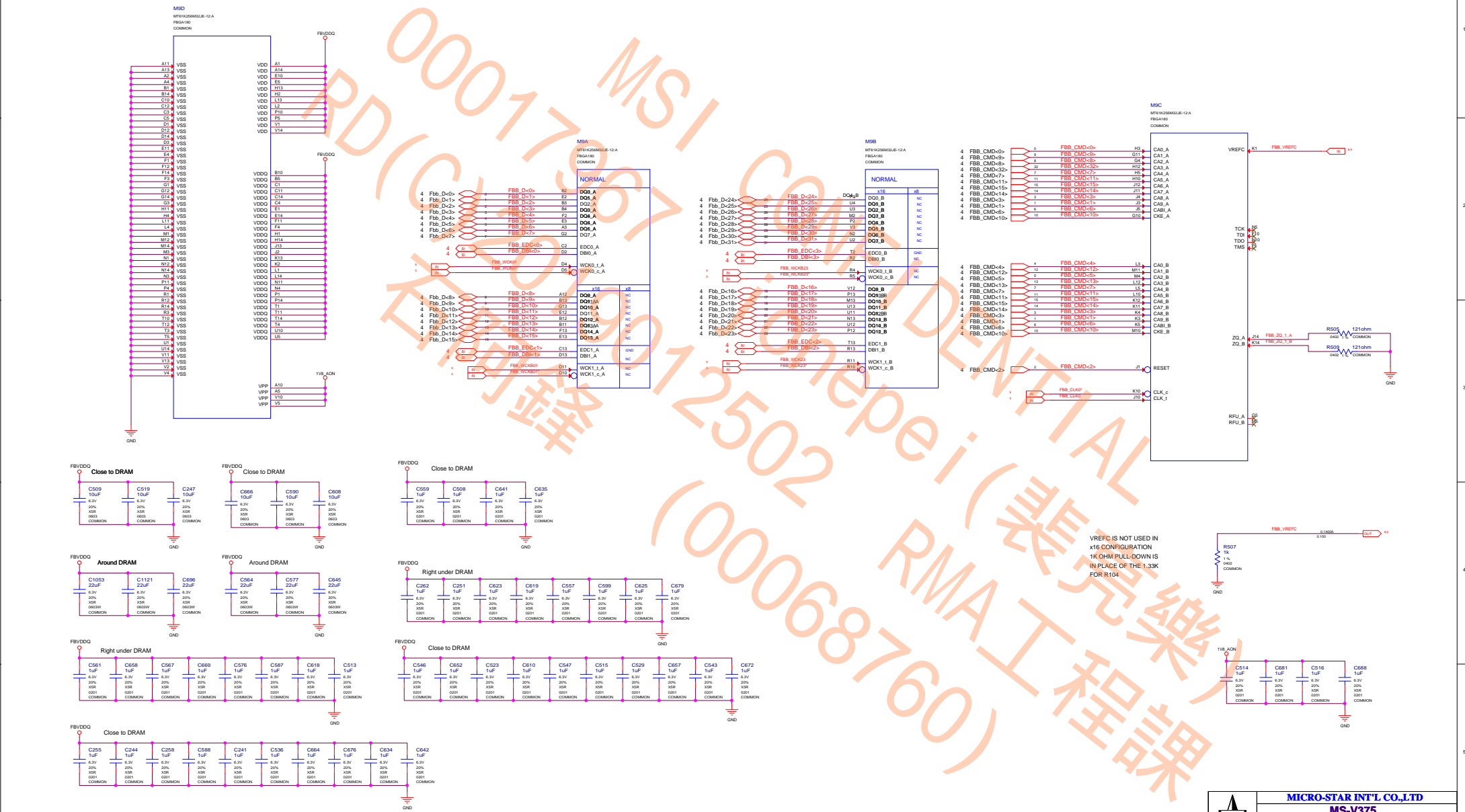
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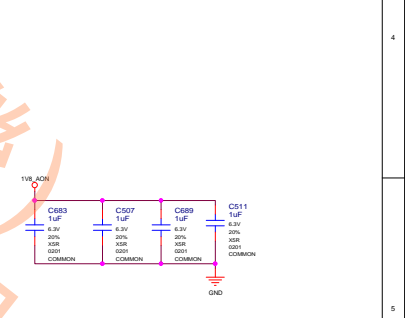
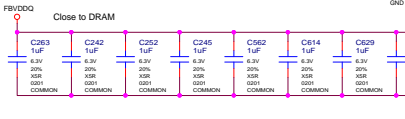
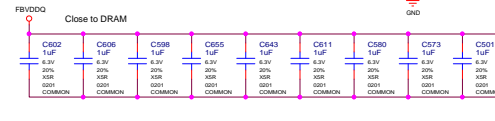
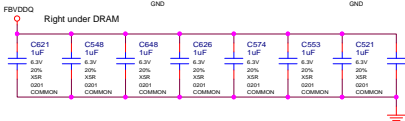
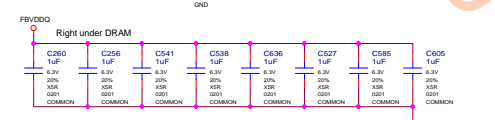
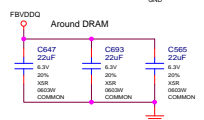
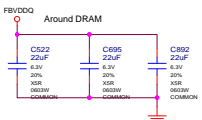
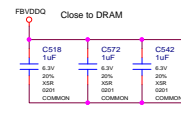
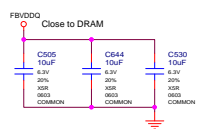
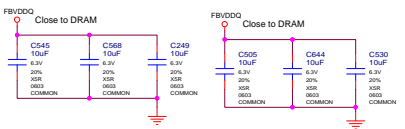
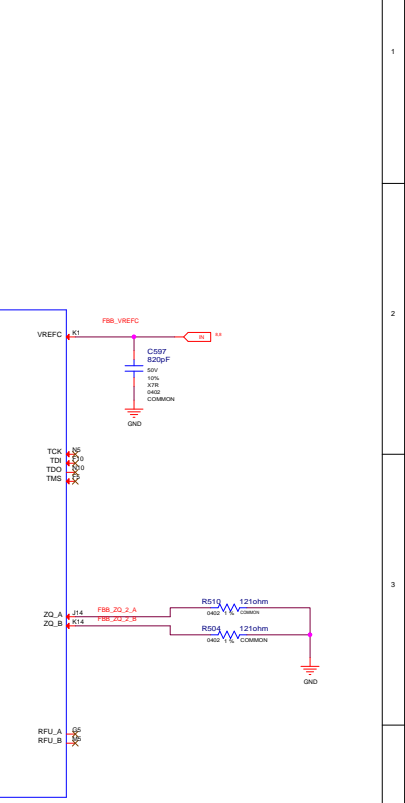
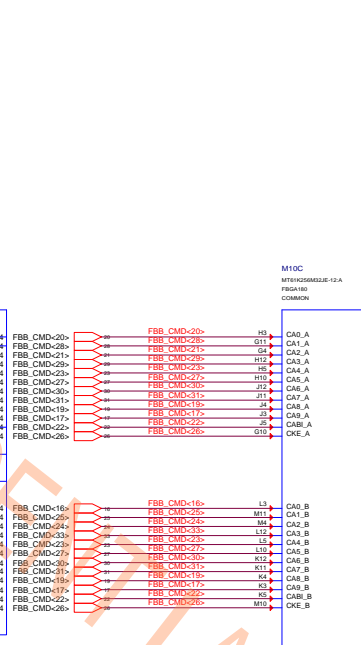
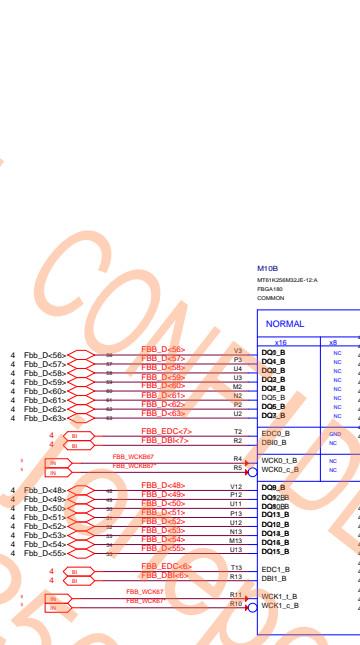
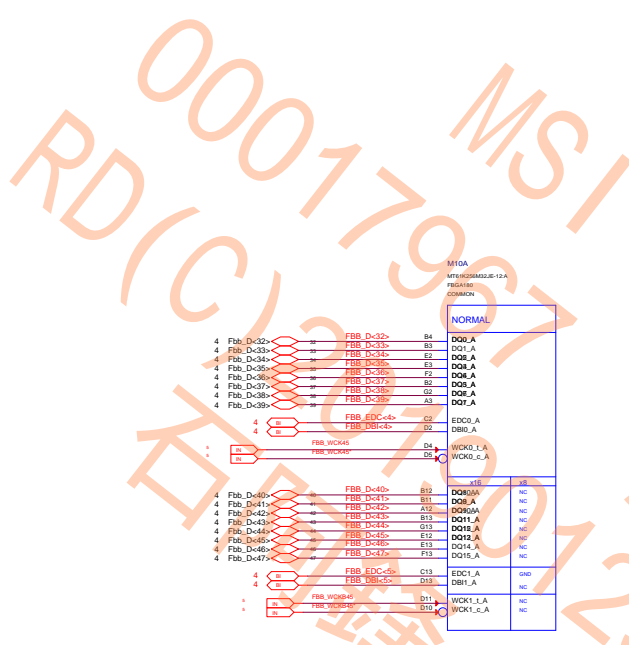
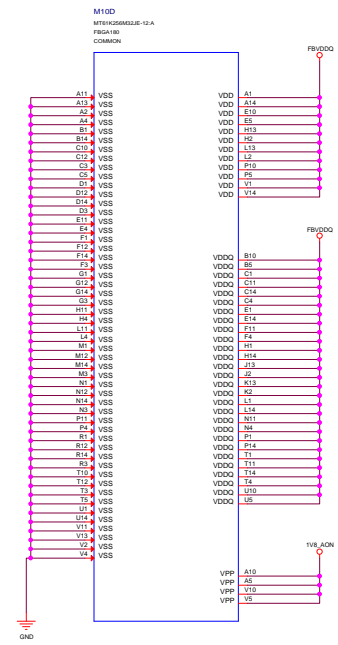


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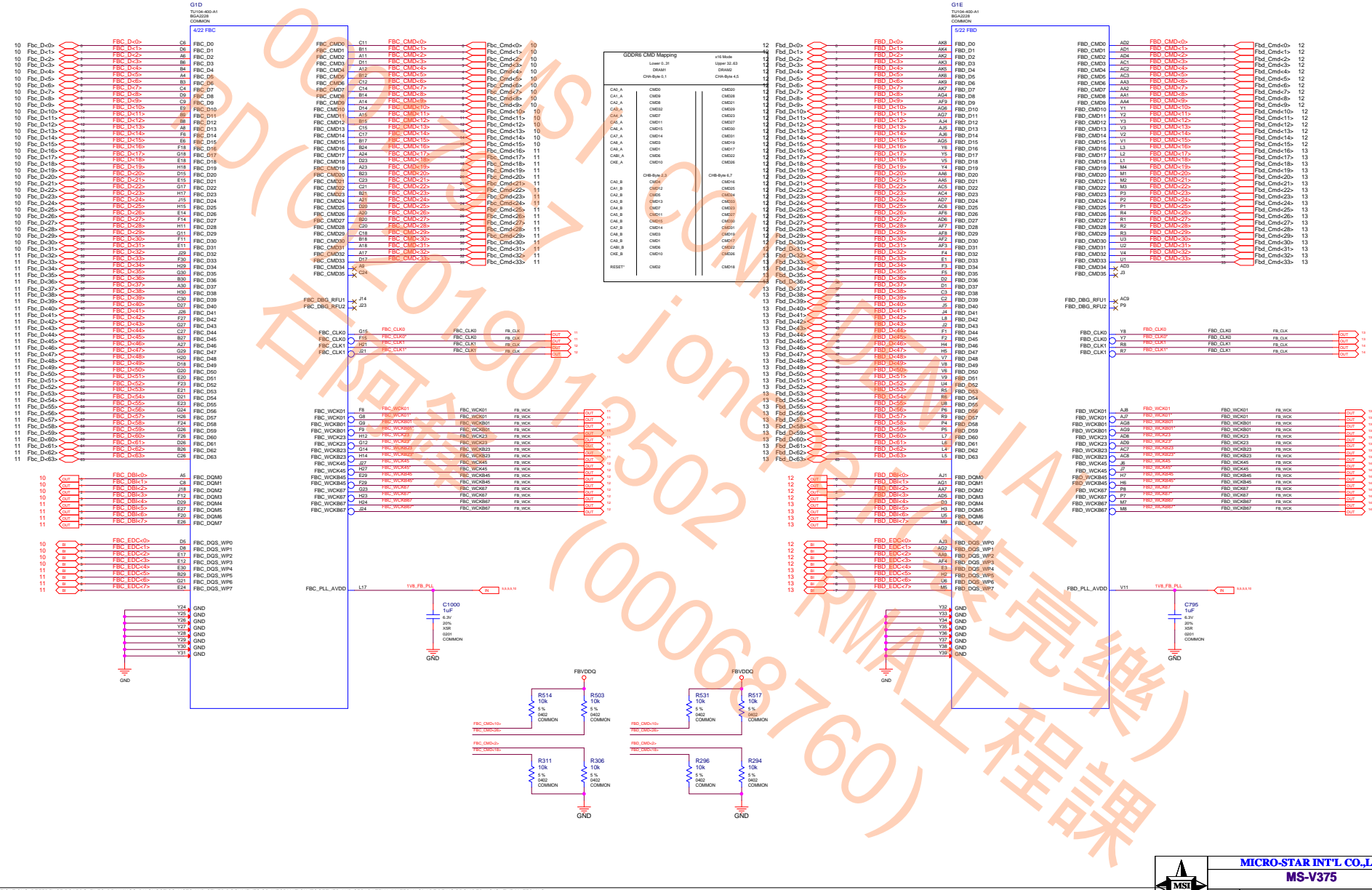
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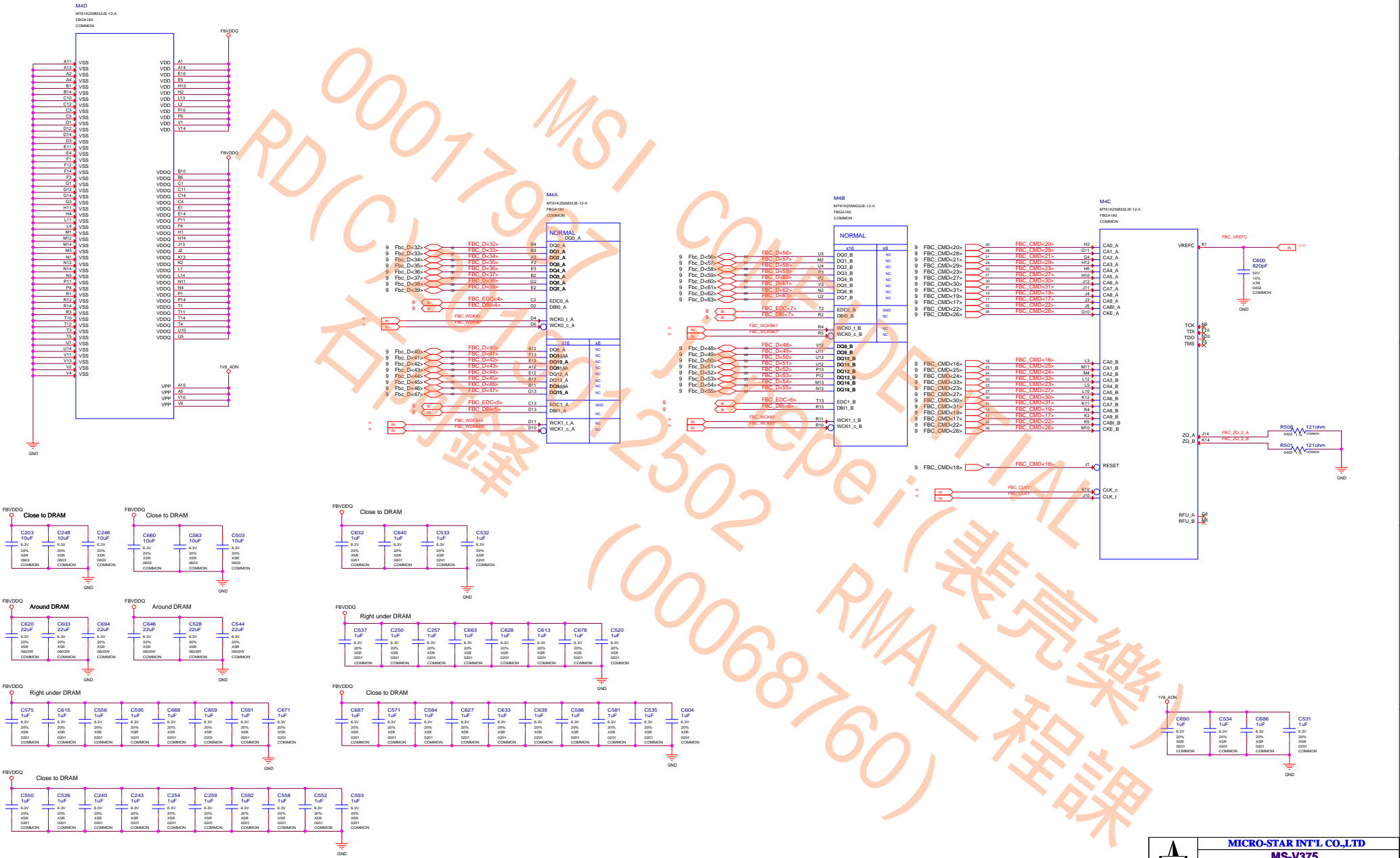
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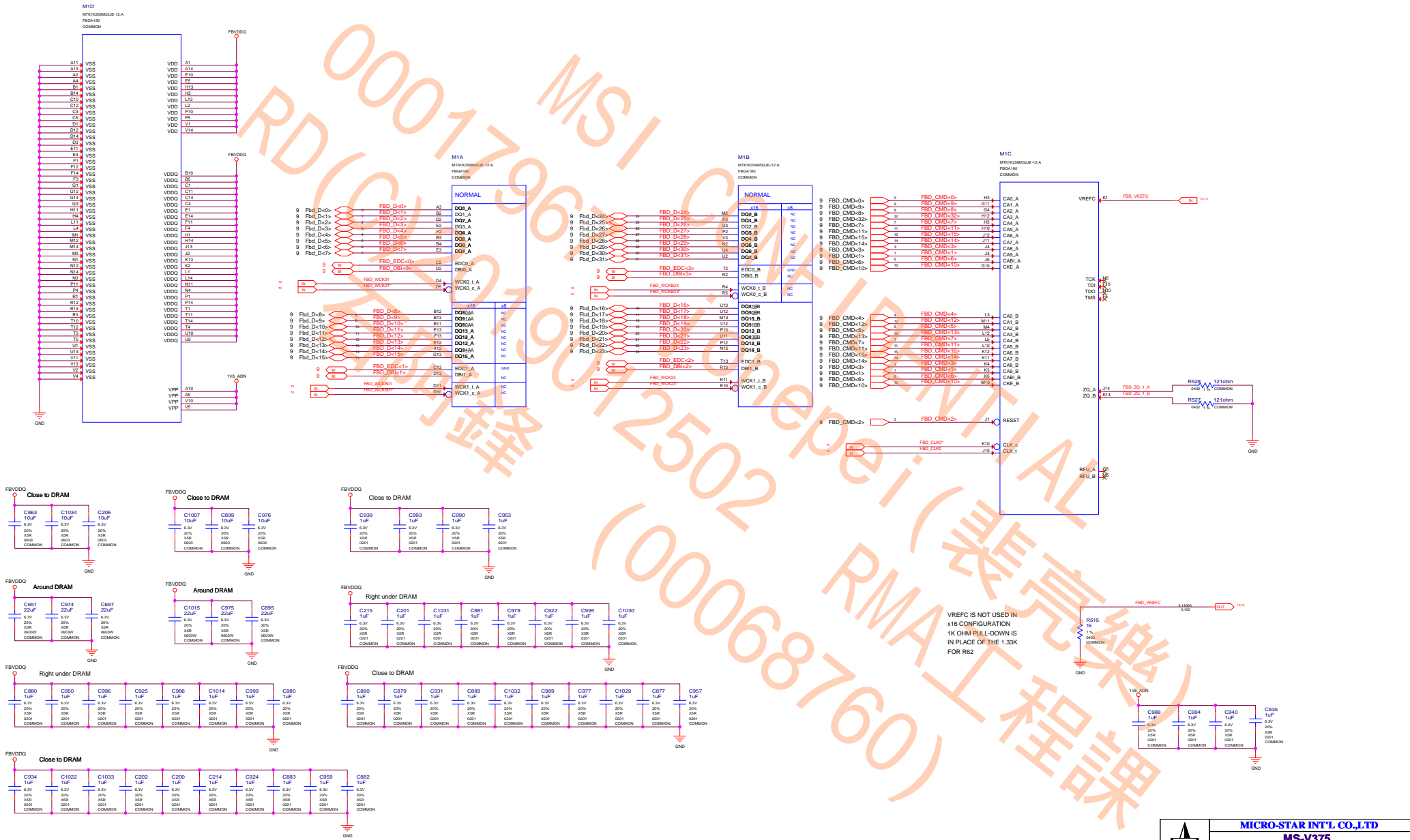
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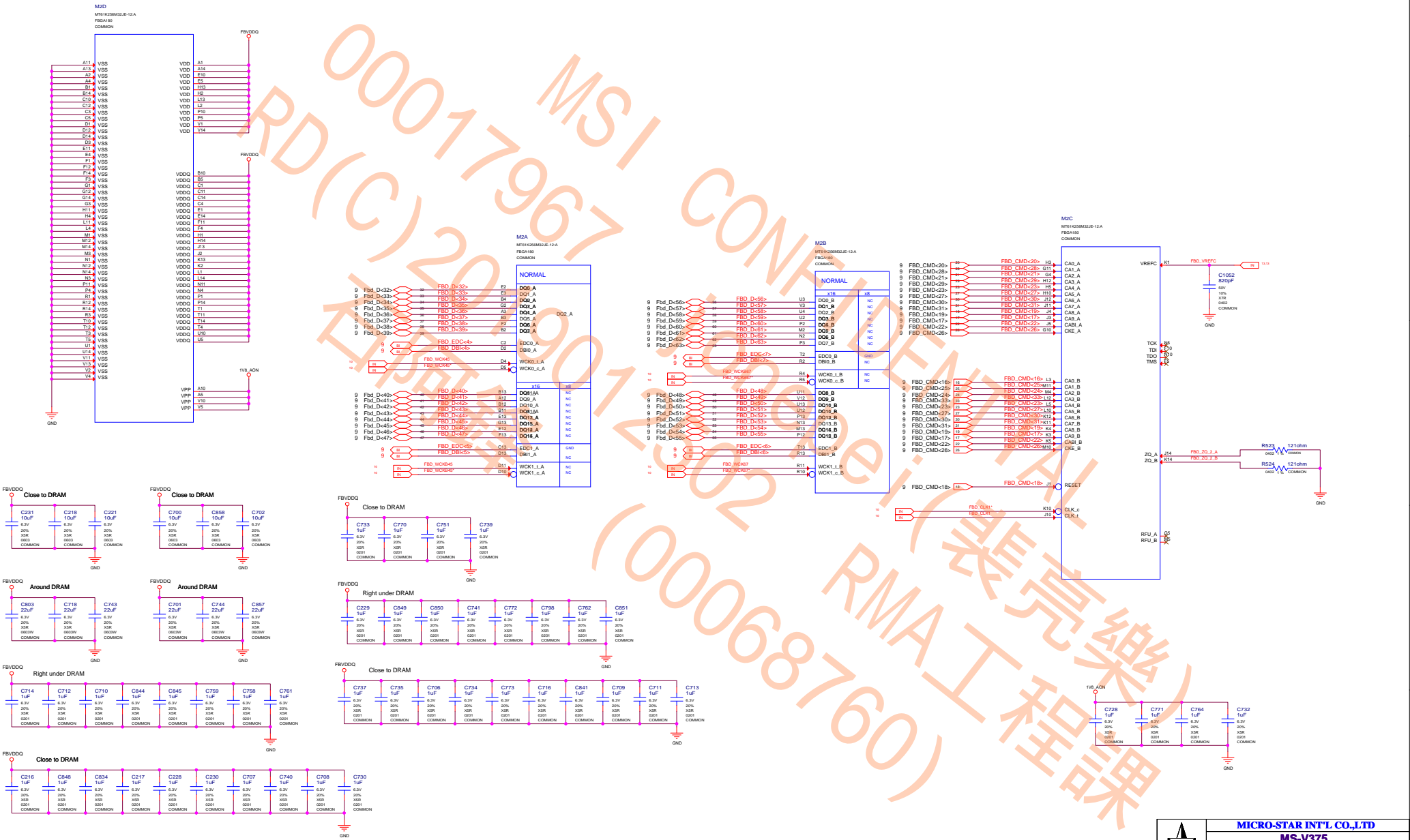
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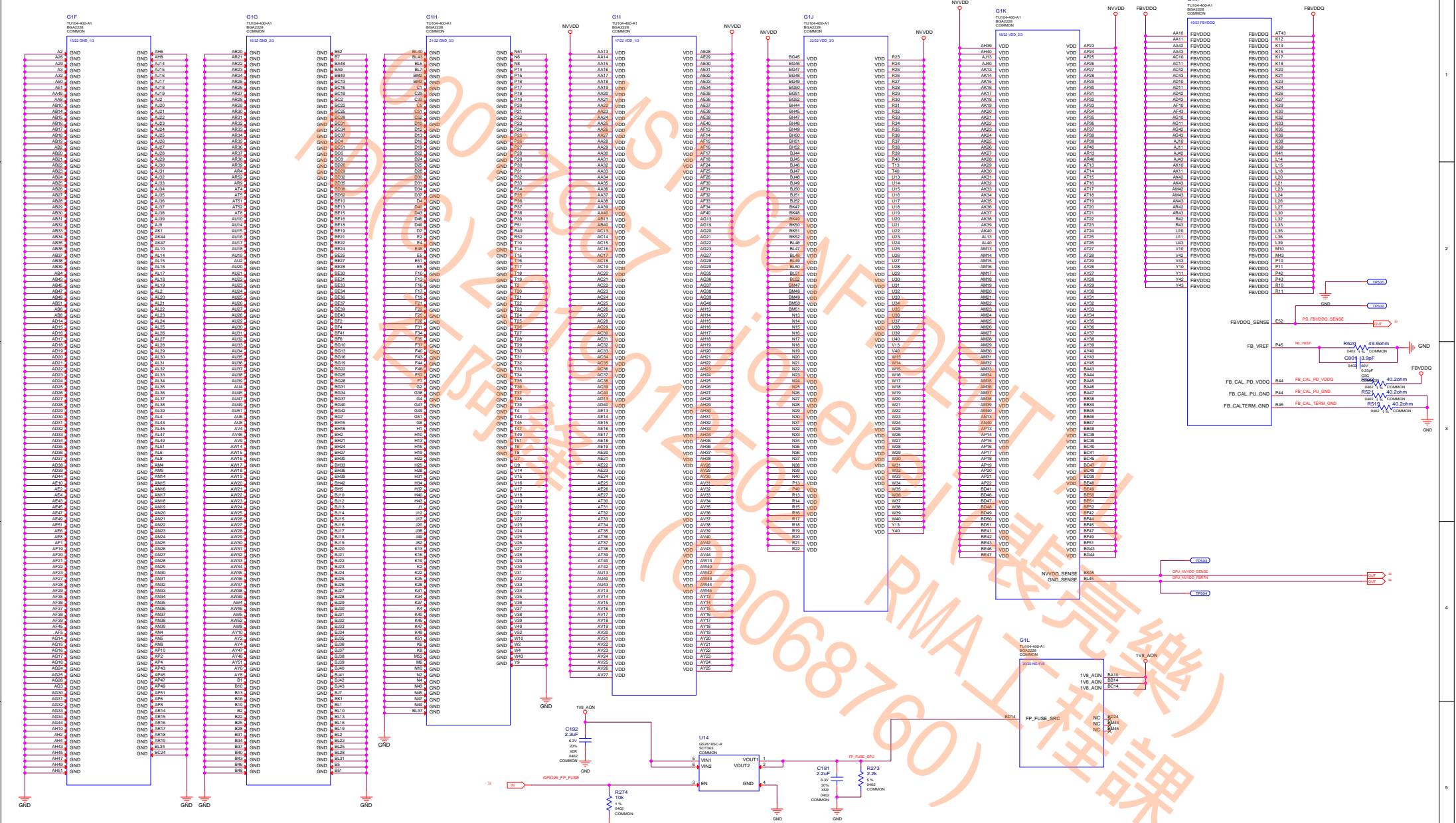
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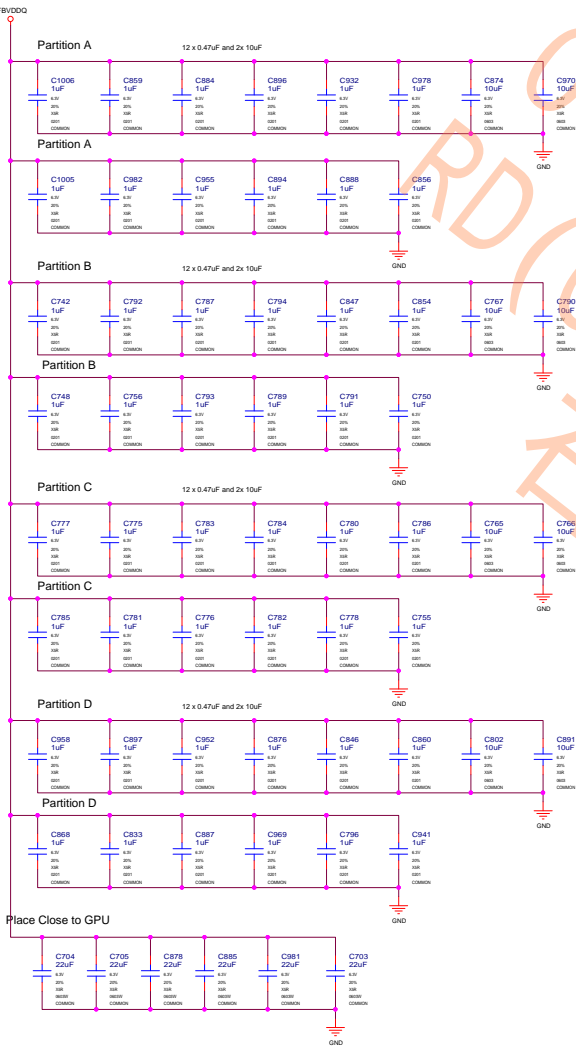
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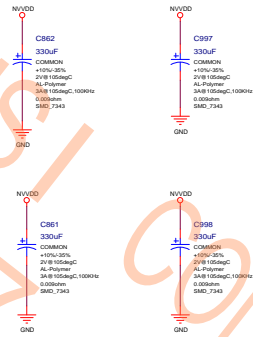
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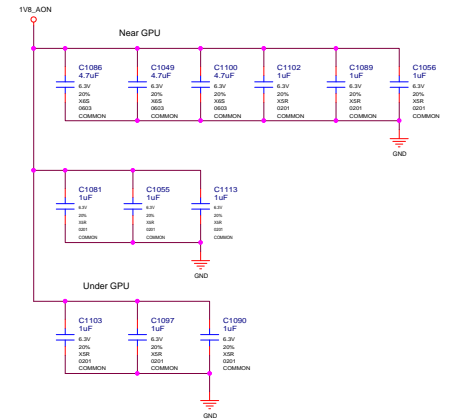
FBVDDQ



NVVDD



1V8_AON



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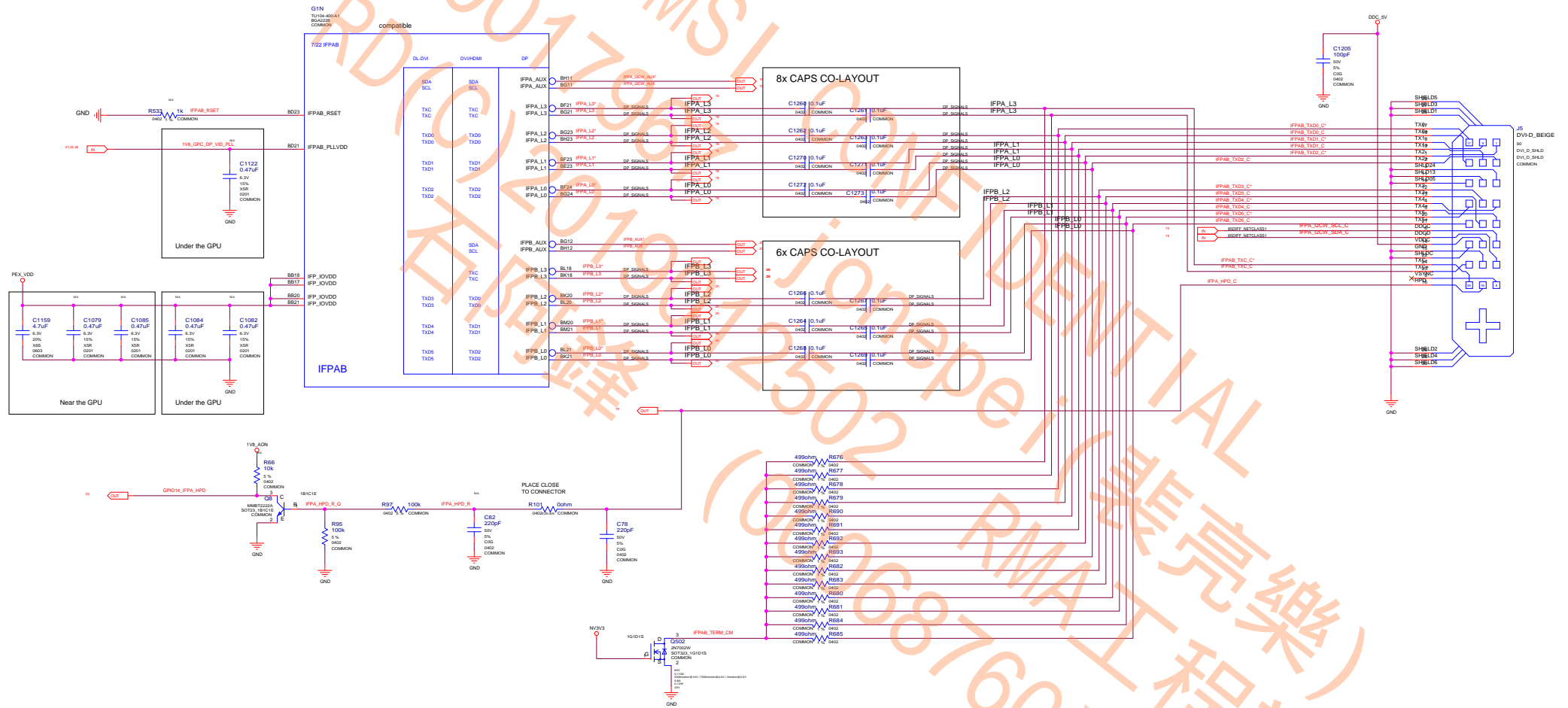
NVDD



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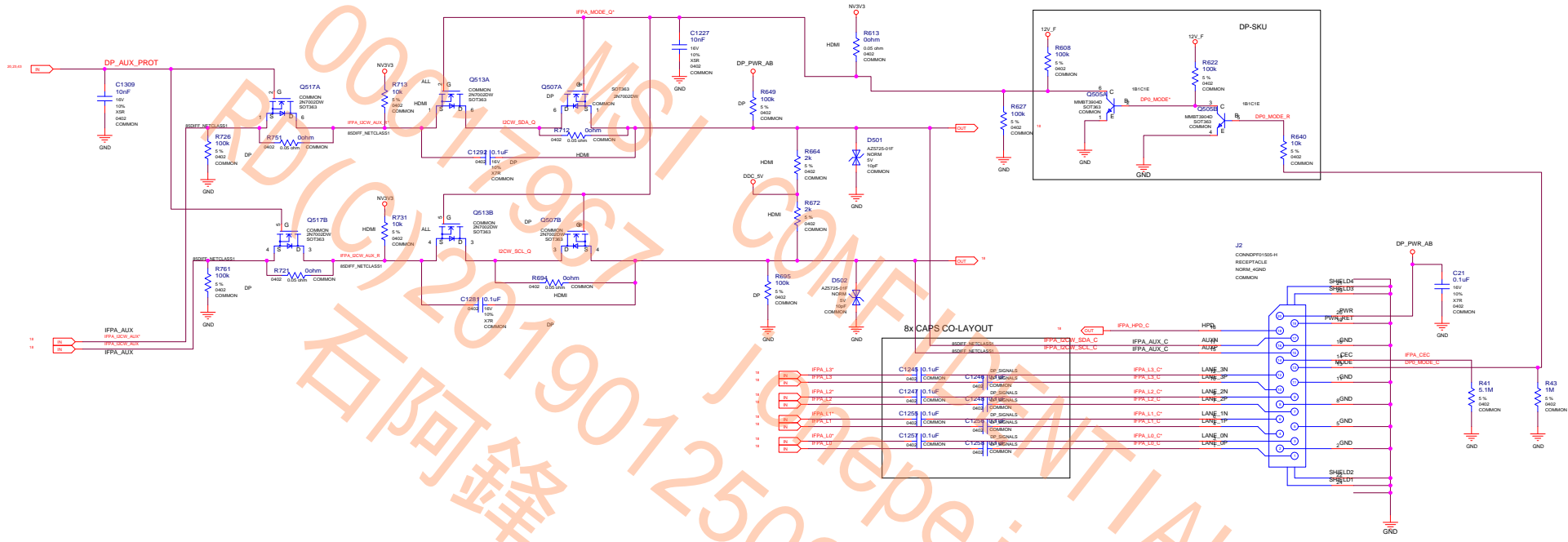
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IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



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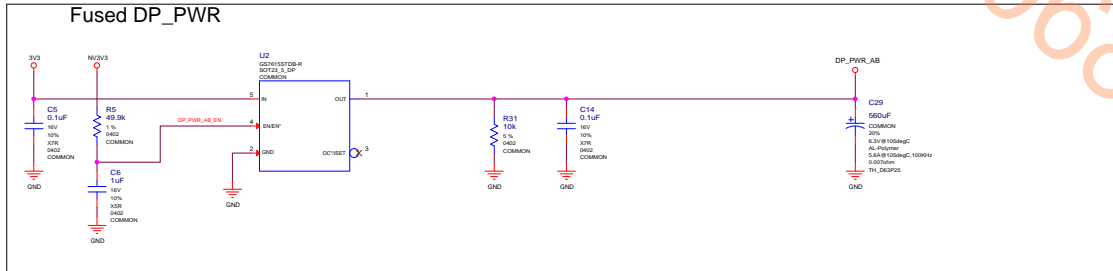
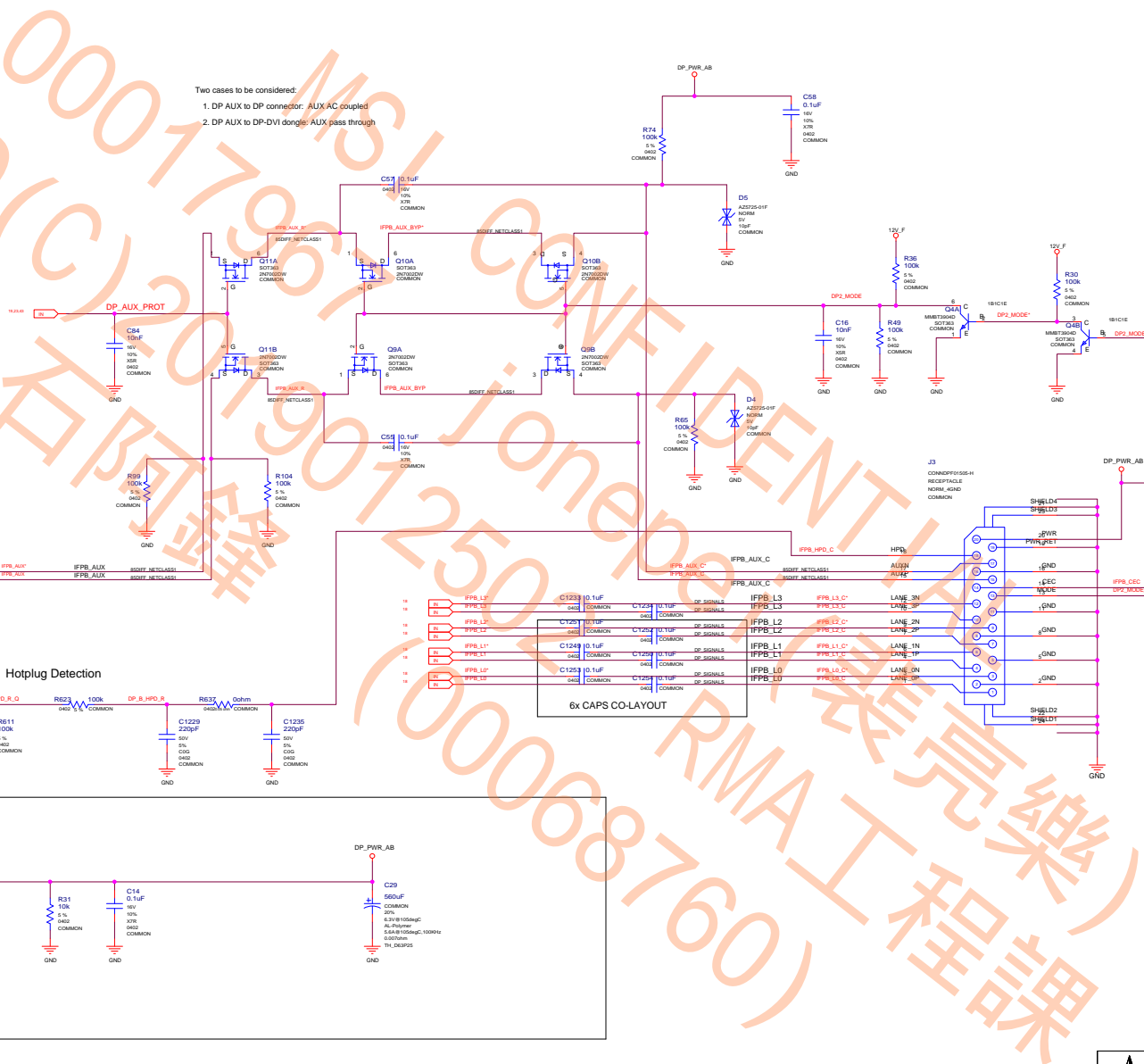
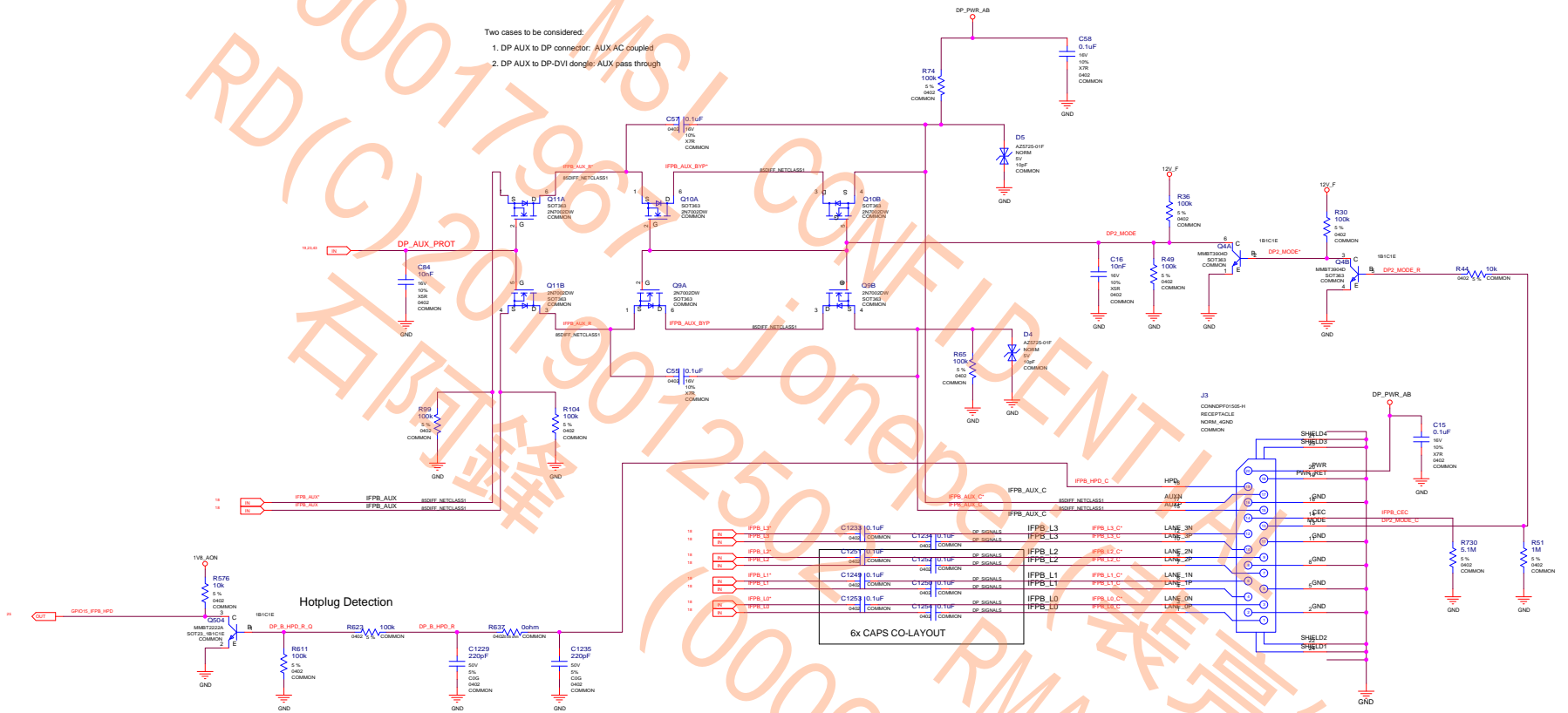
IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

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IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

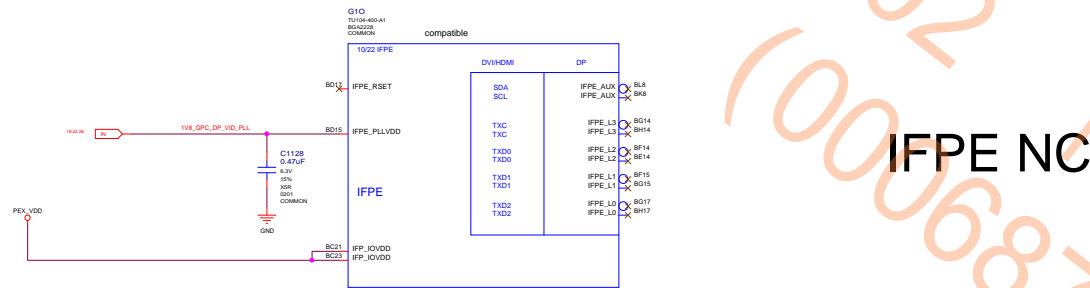
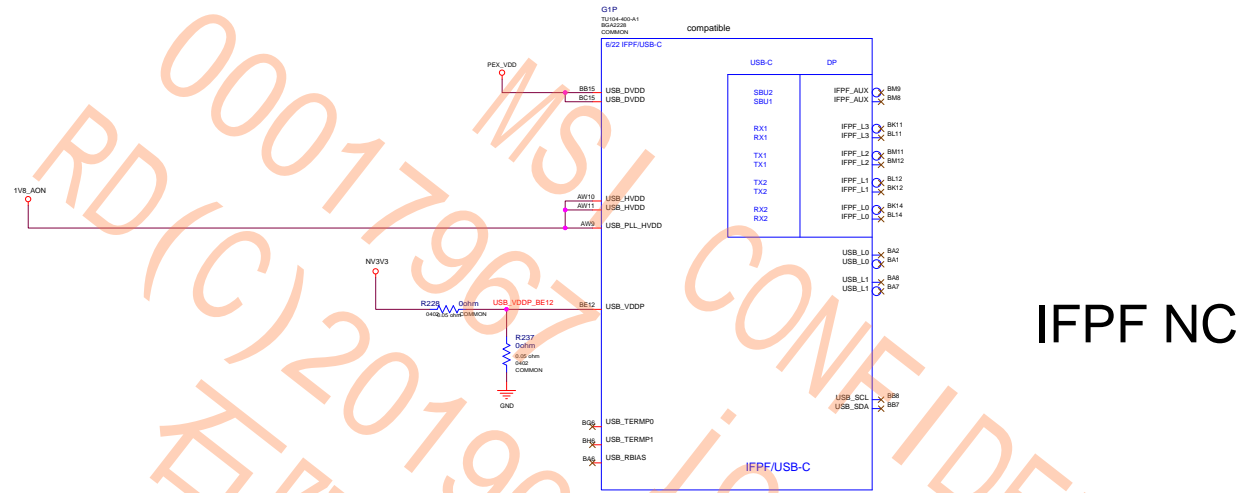


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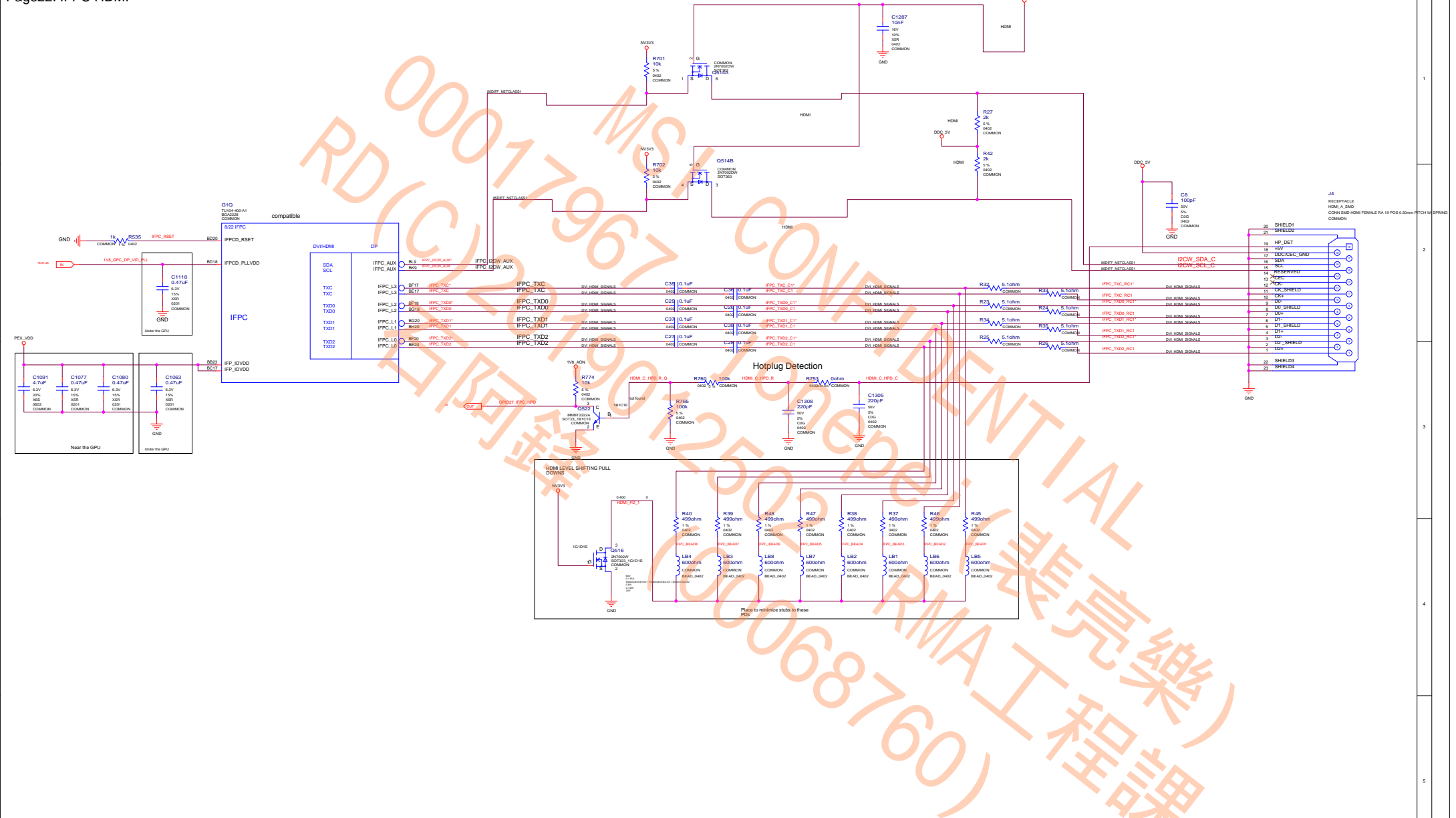
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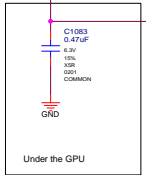
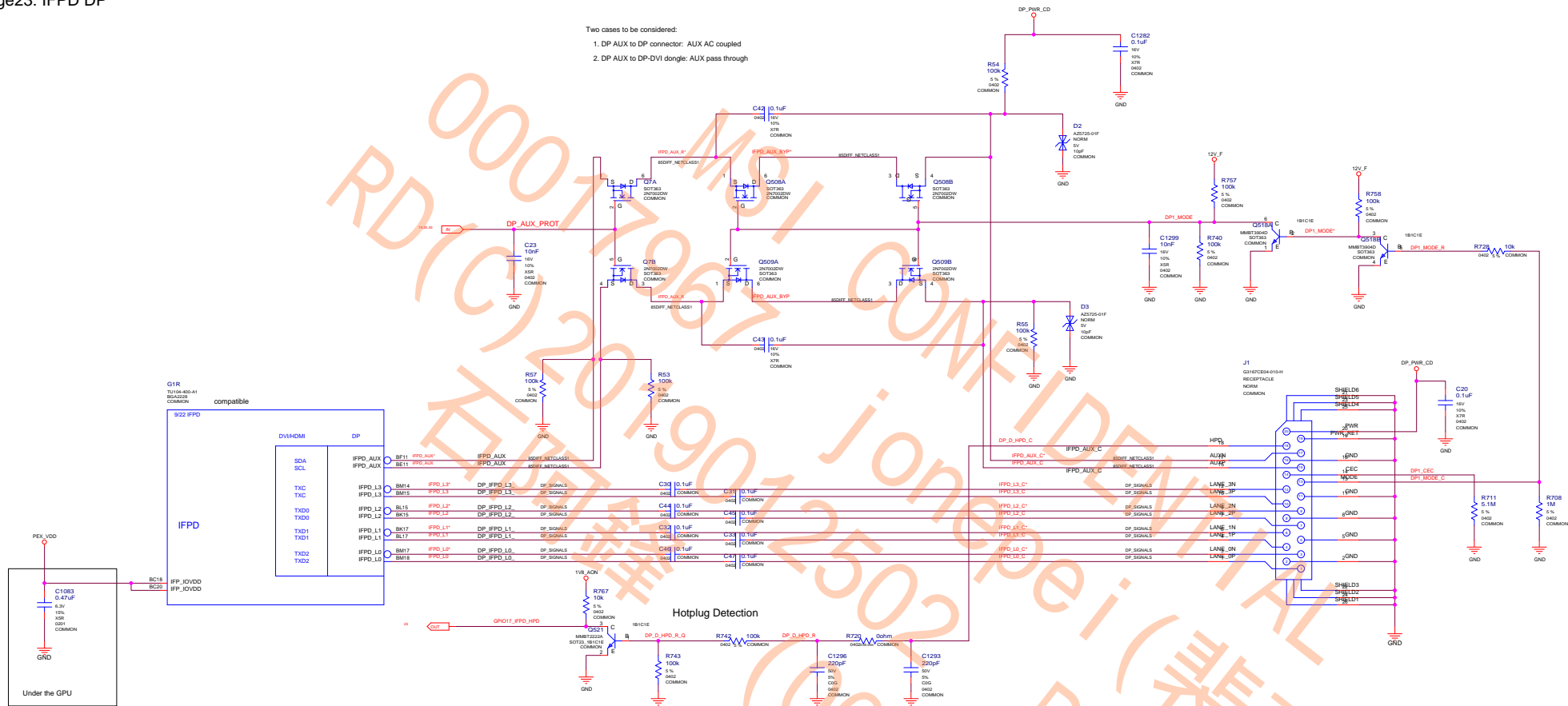
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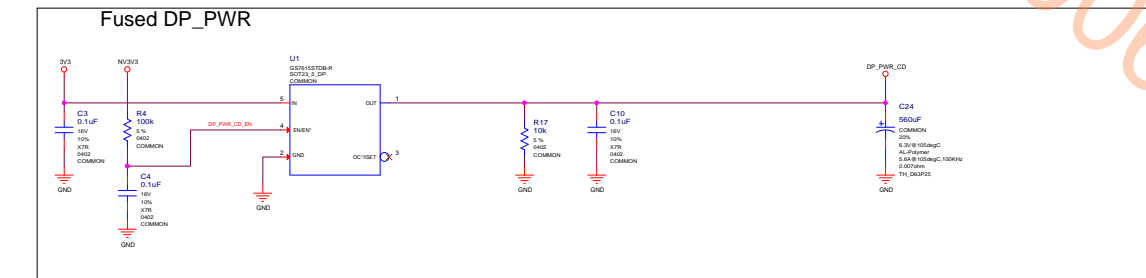
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Two cases to be considered:
 1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

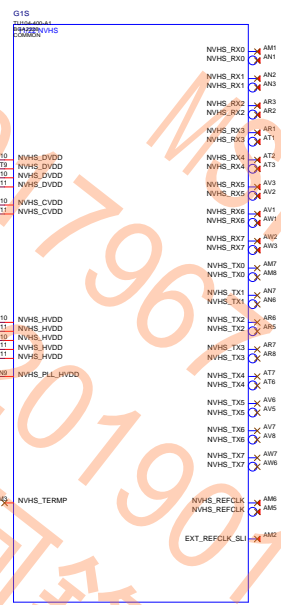


Hotplug Detection

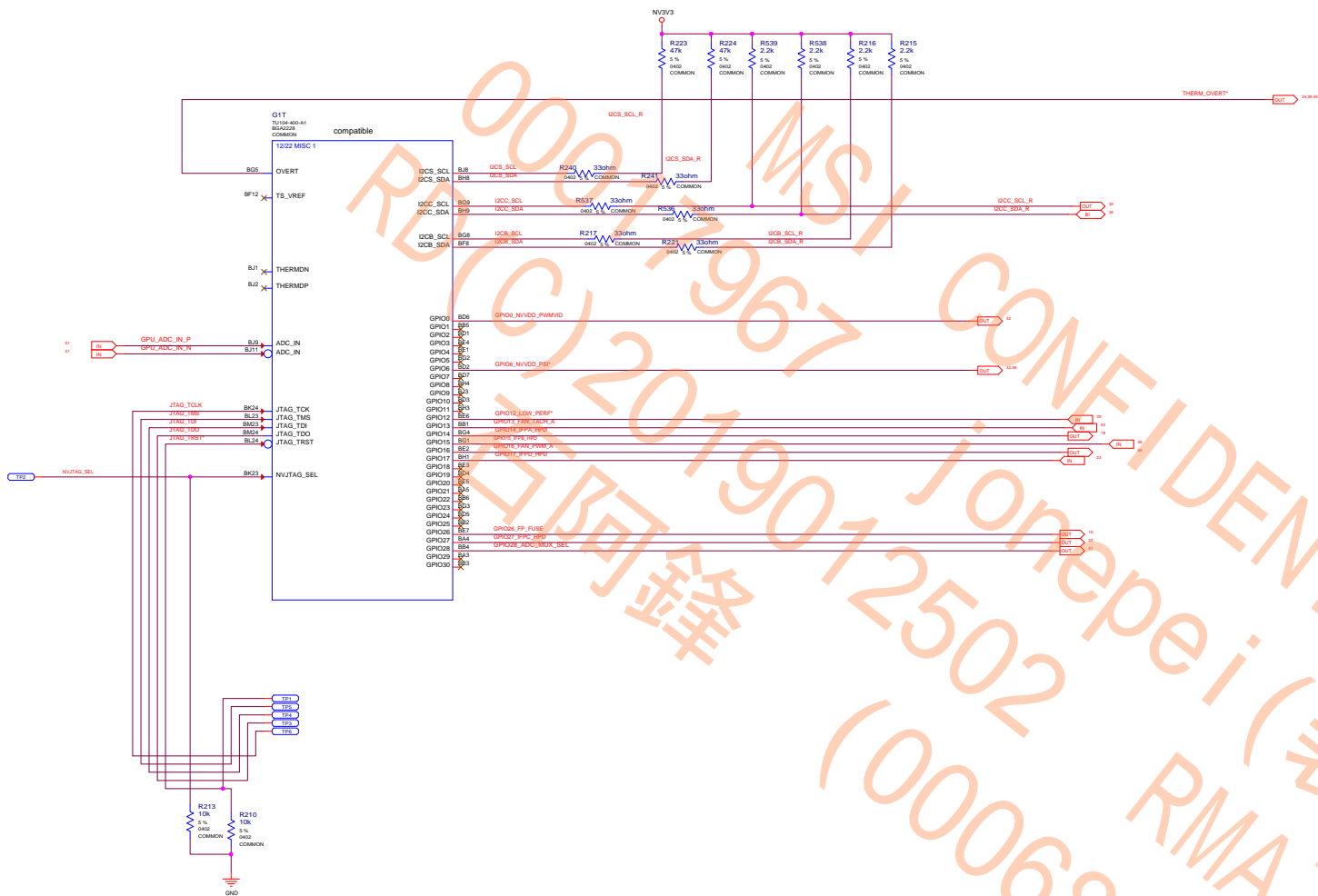


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 石阿鋒 jonepei (裴亮樂)
 (00068760) RMA 工程師



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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

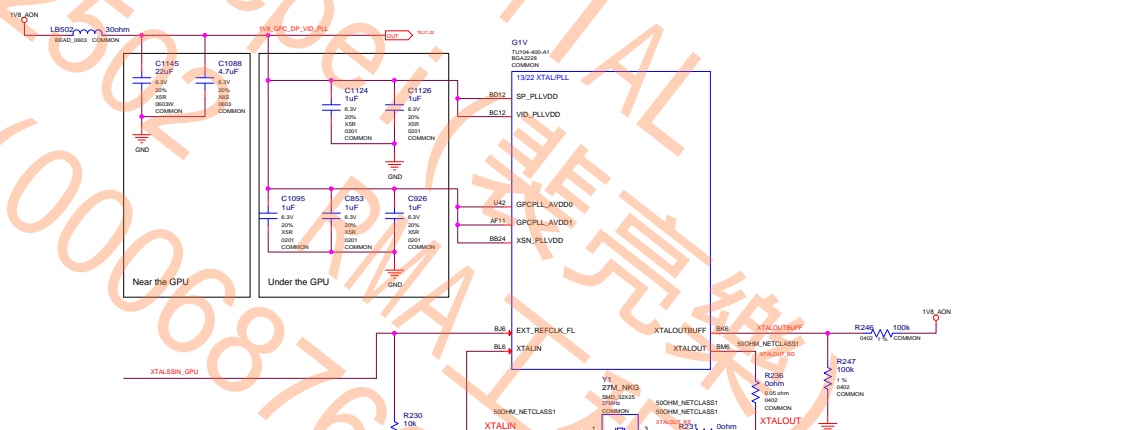
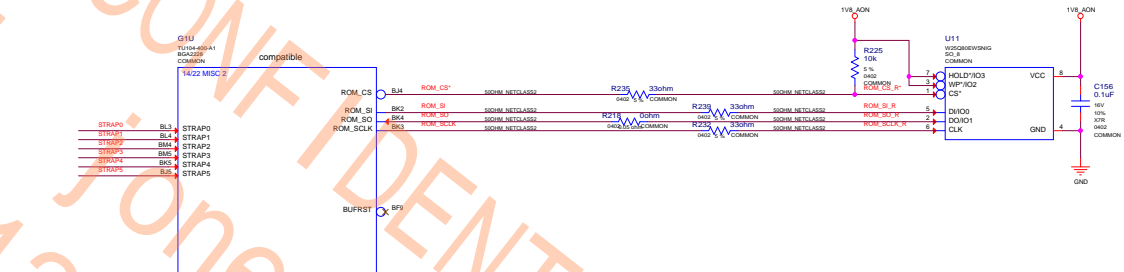
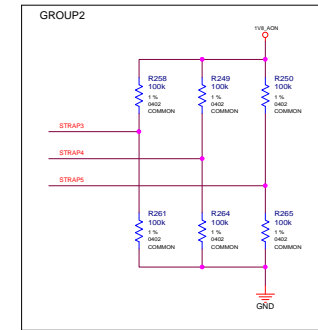
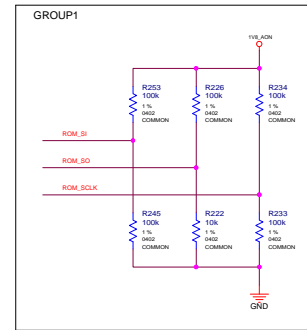
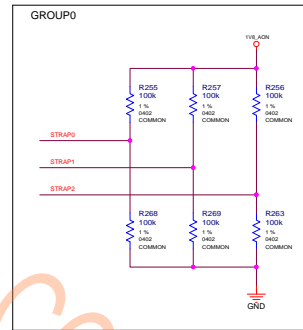
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



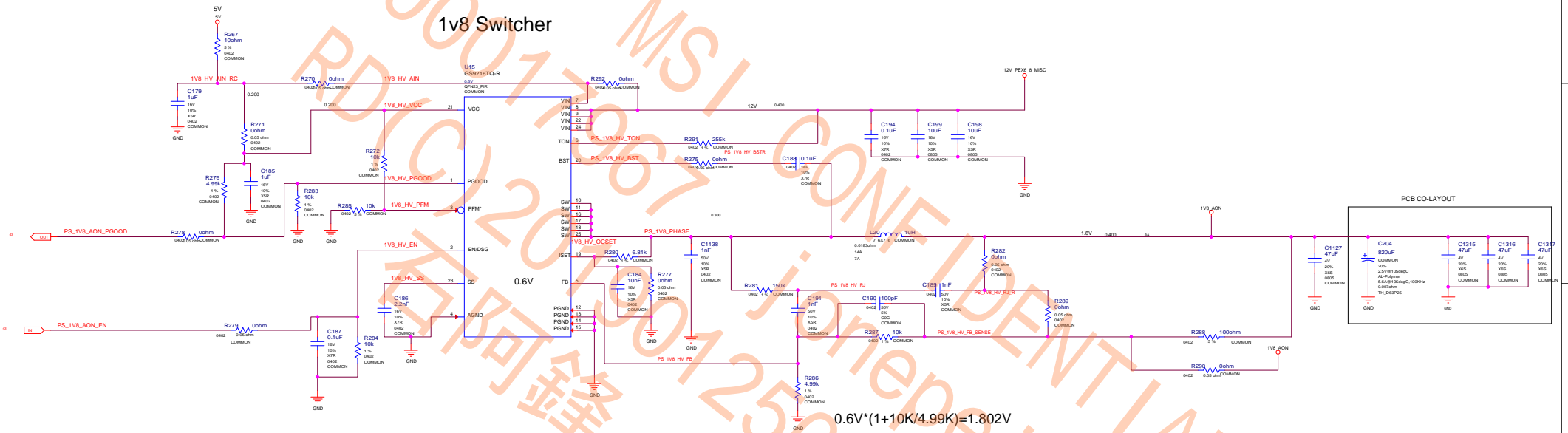
XTALOUTBUFF	
1.8V	0V
50% PWM	DISABLED (100%)

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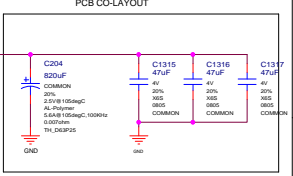
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1v8 Switcher

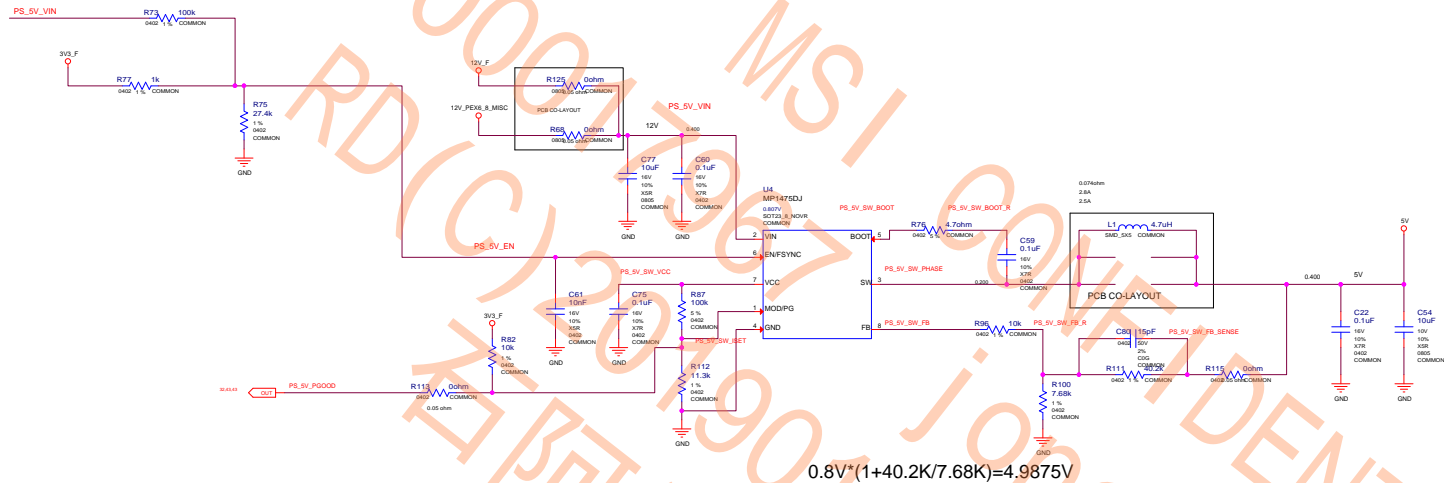


$$0.6V * (1 + 10K / 4.99K) = 1.802V$$



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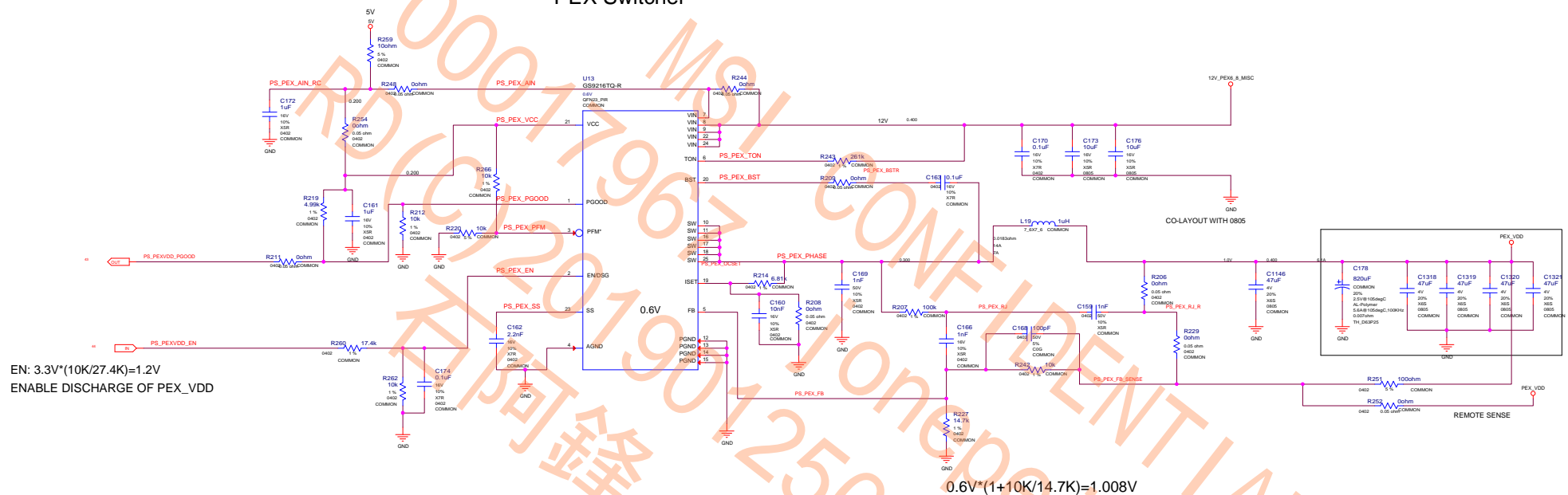


$$0.8V \cdot (1 + 40.2K / 7.68K) = 4.9875V$$

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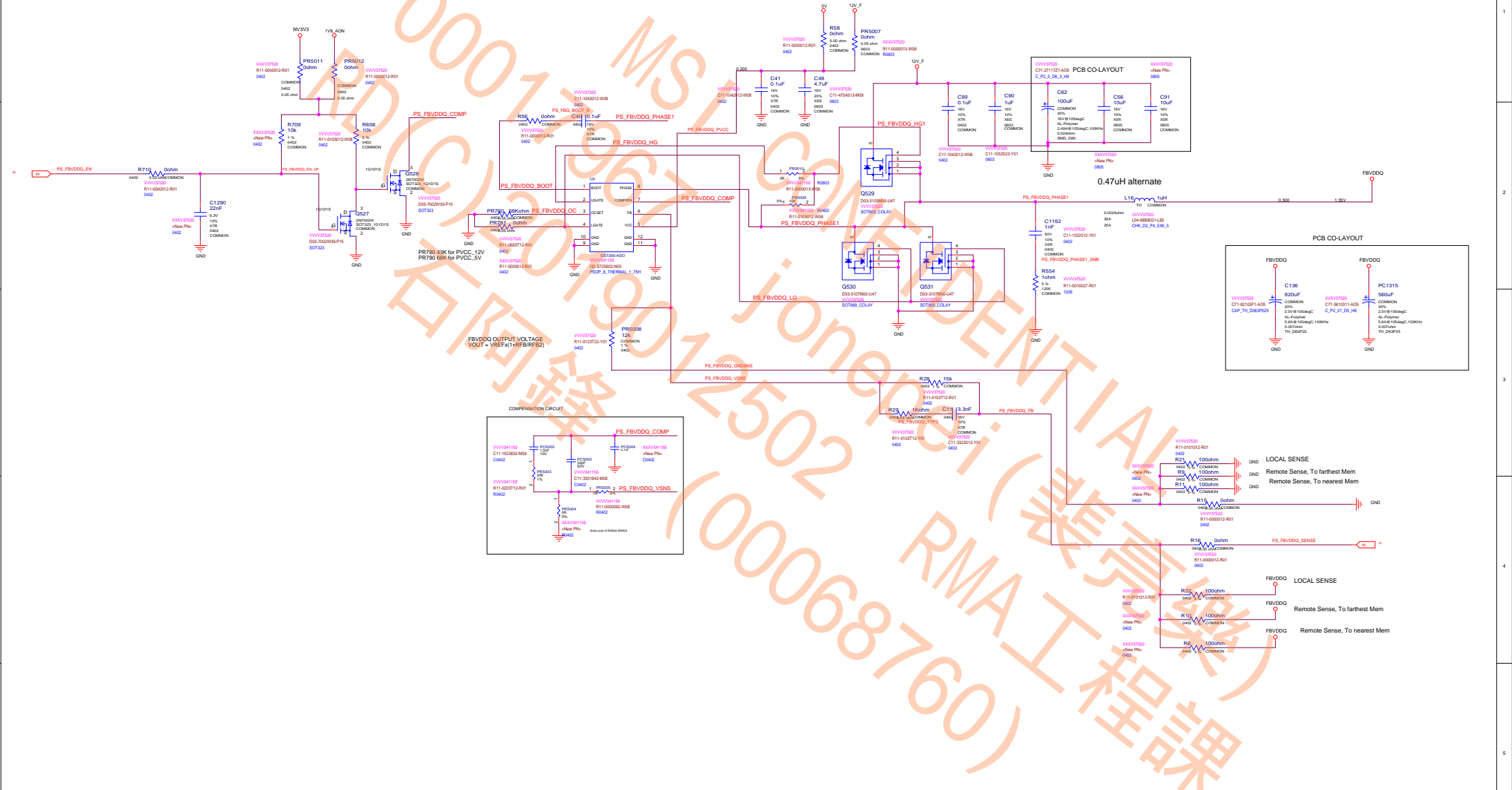
PEX Switcher



EN: $3.3V * (10K/27.4K) = 1.2V$
 ENABLE DISCHARGE OF PEX_VDD

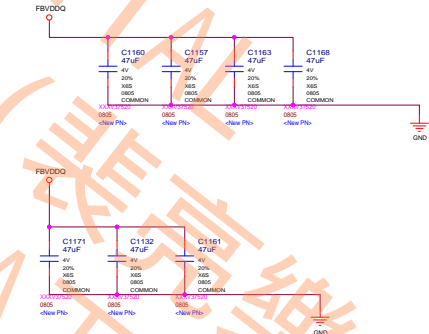
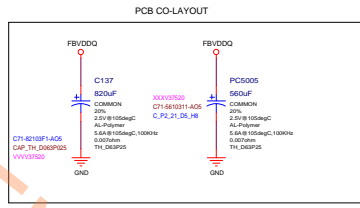
$0.6V * (1 + 10K/14.7K) = 1.008V$

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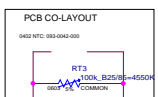
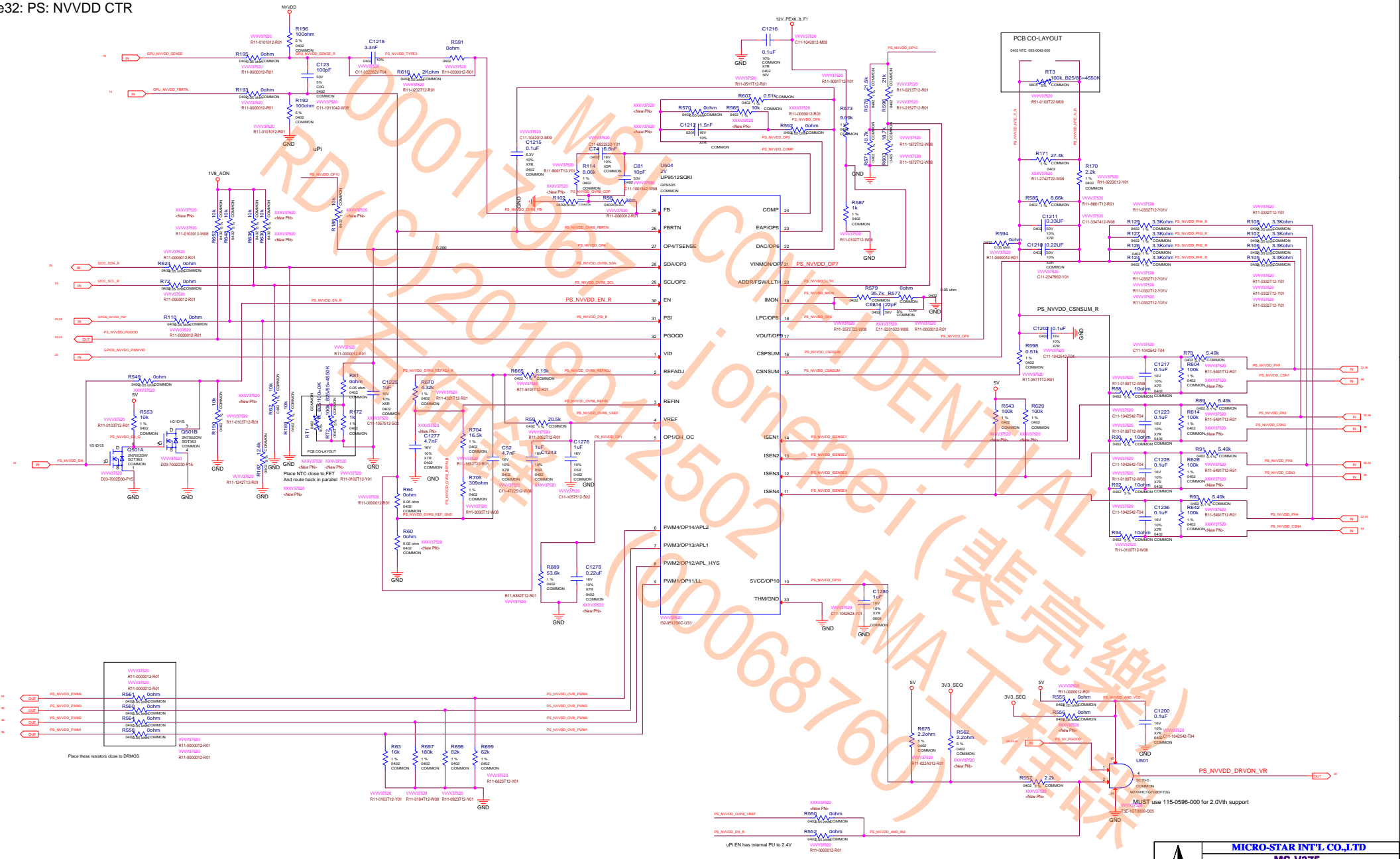
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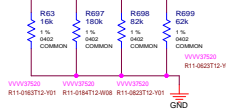


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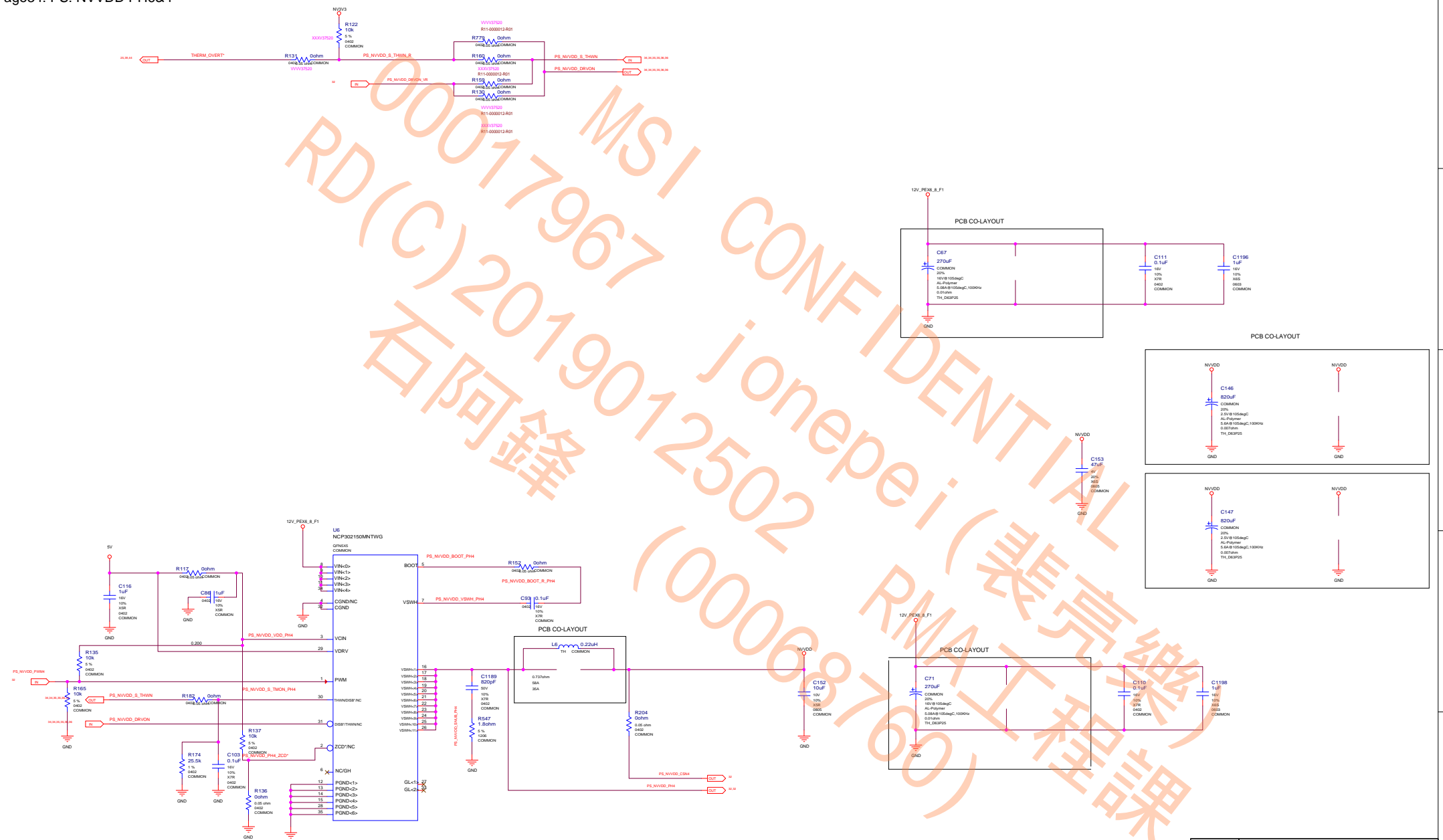
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DROP OVR3i SOLUTION

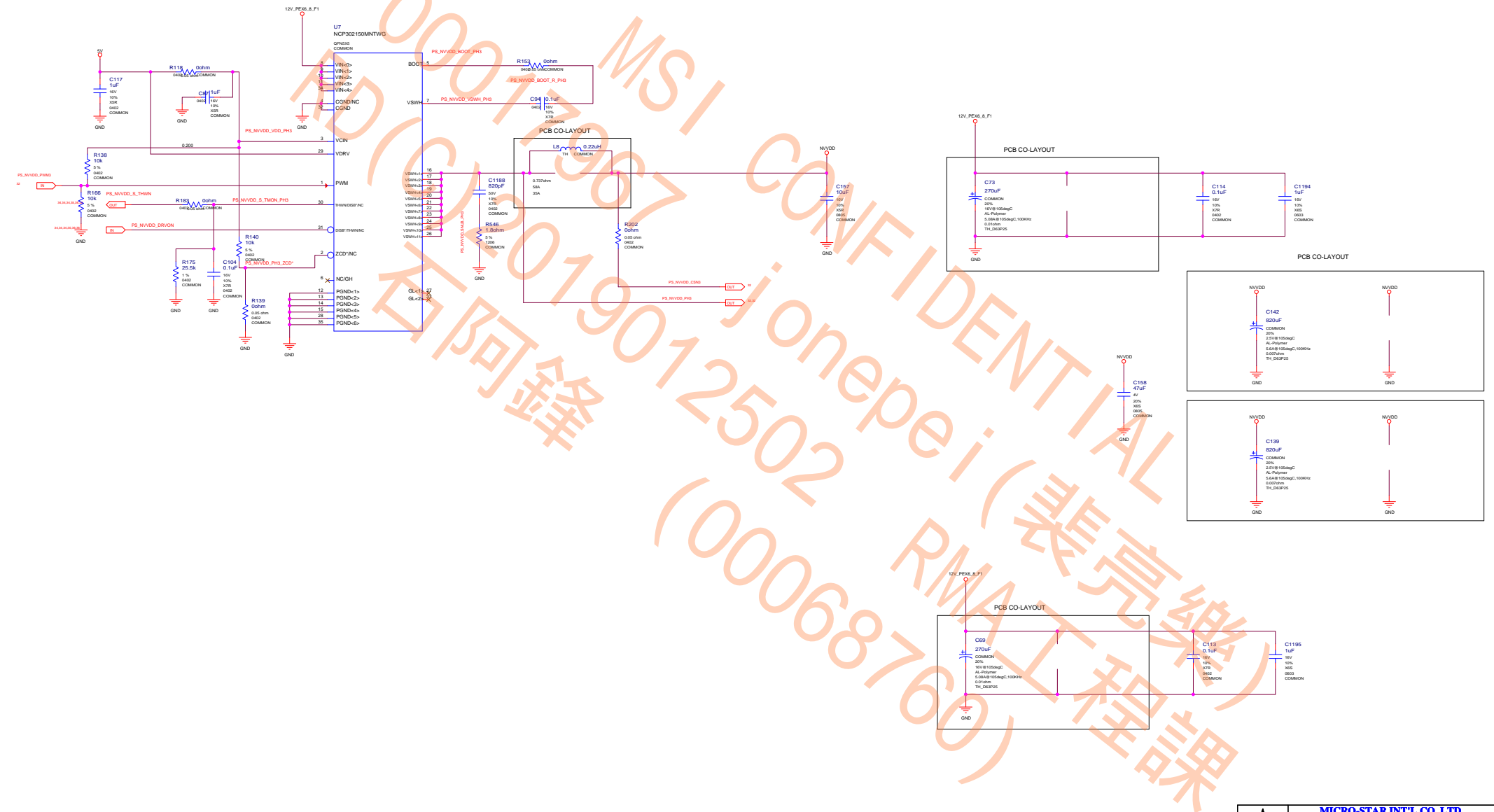
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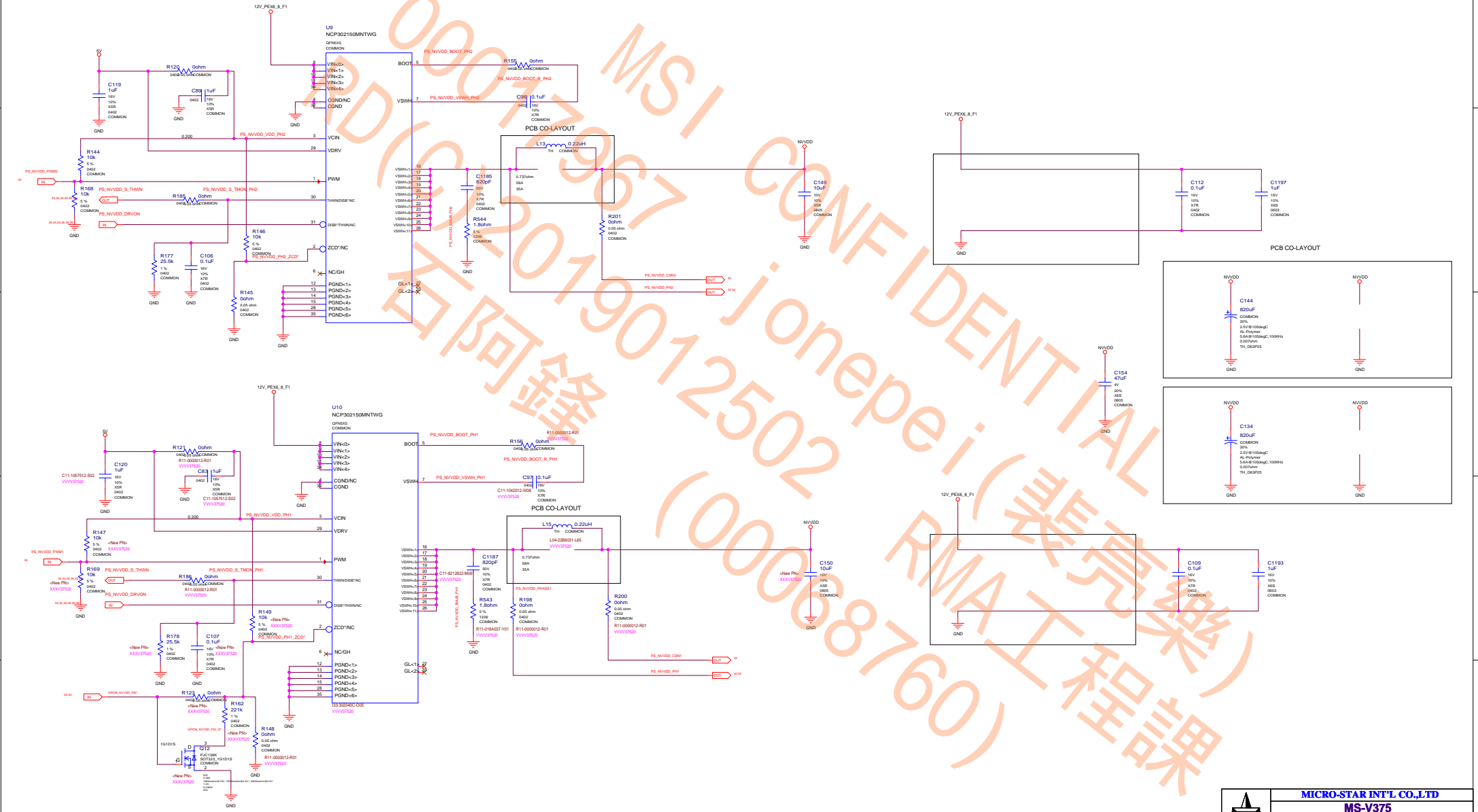
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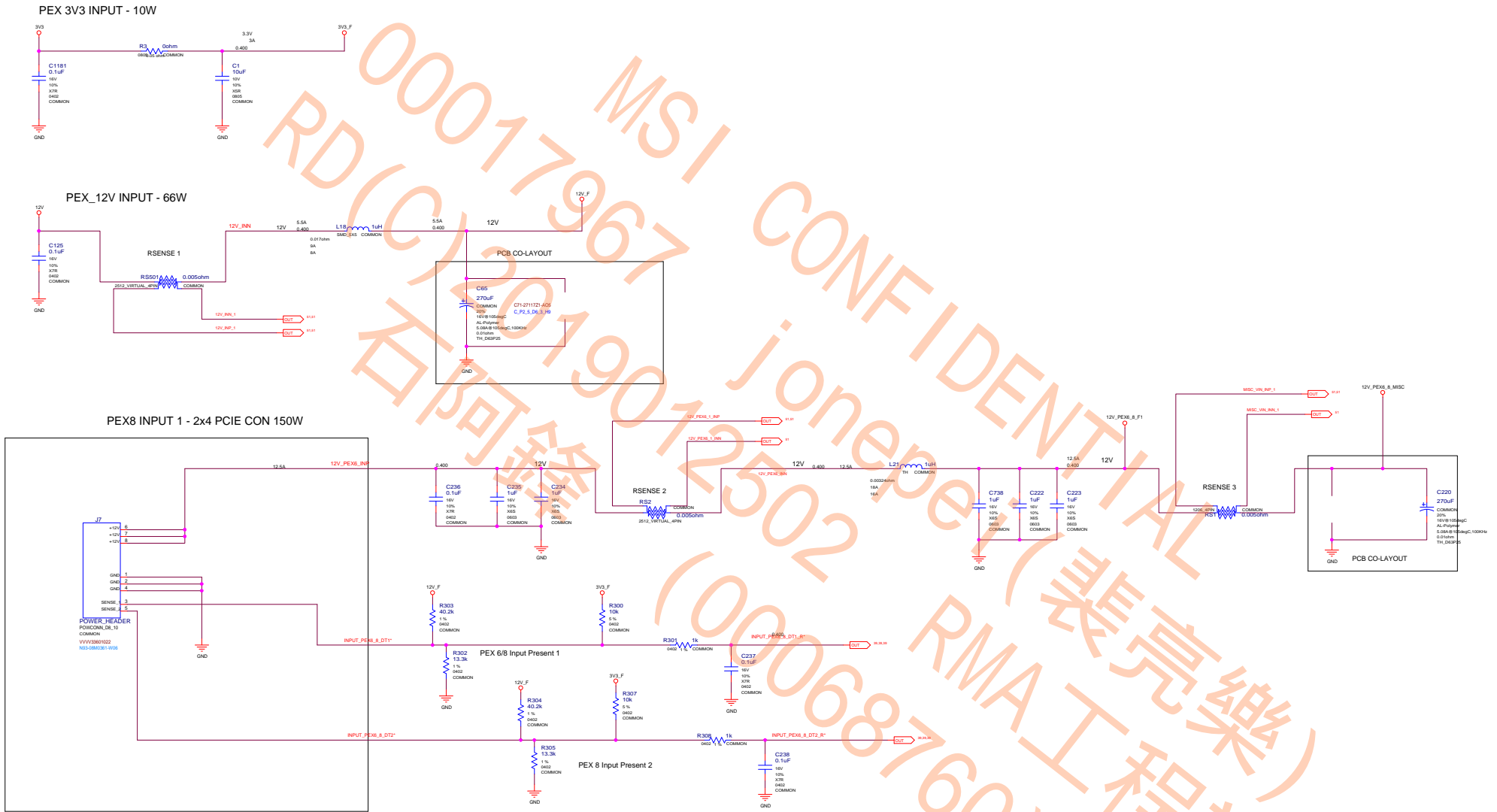
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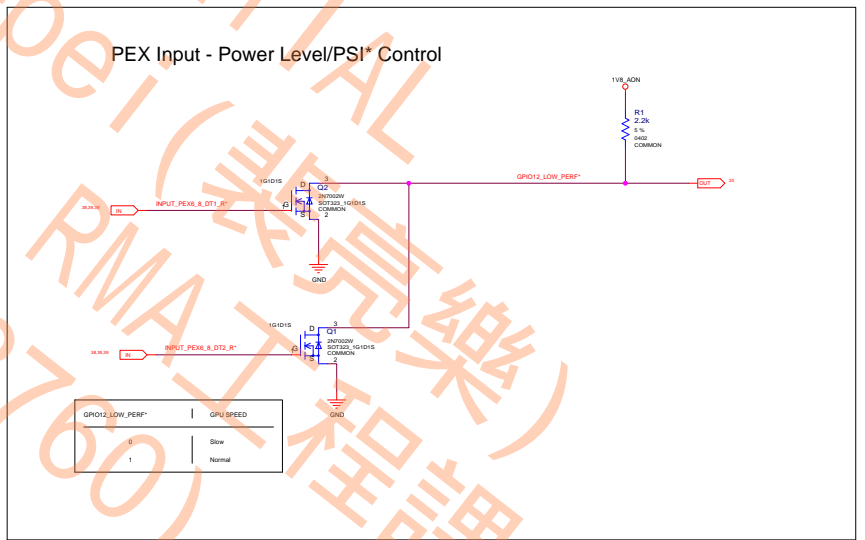
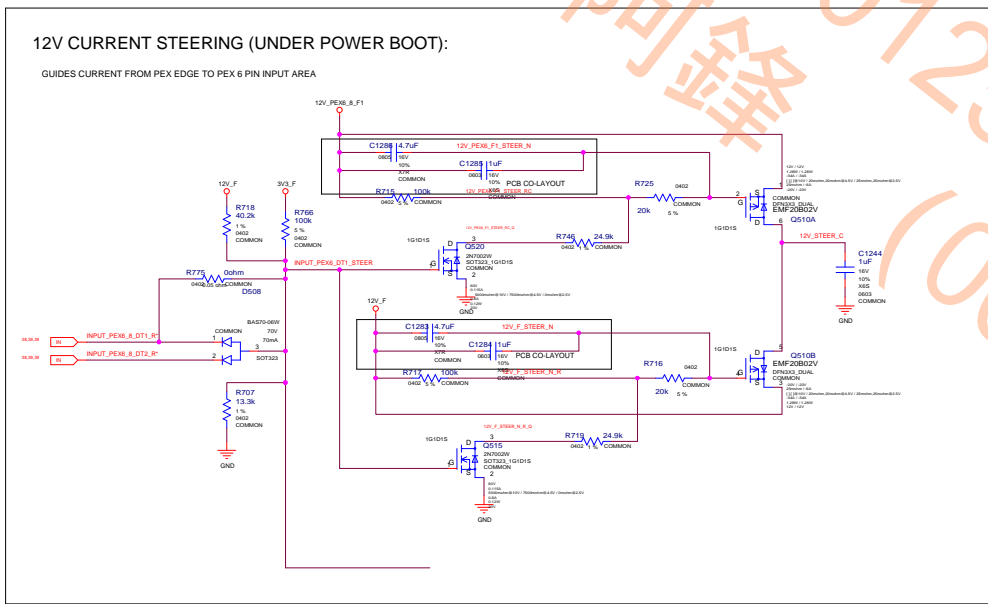
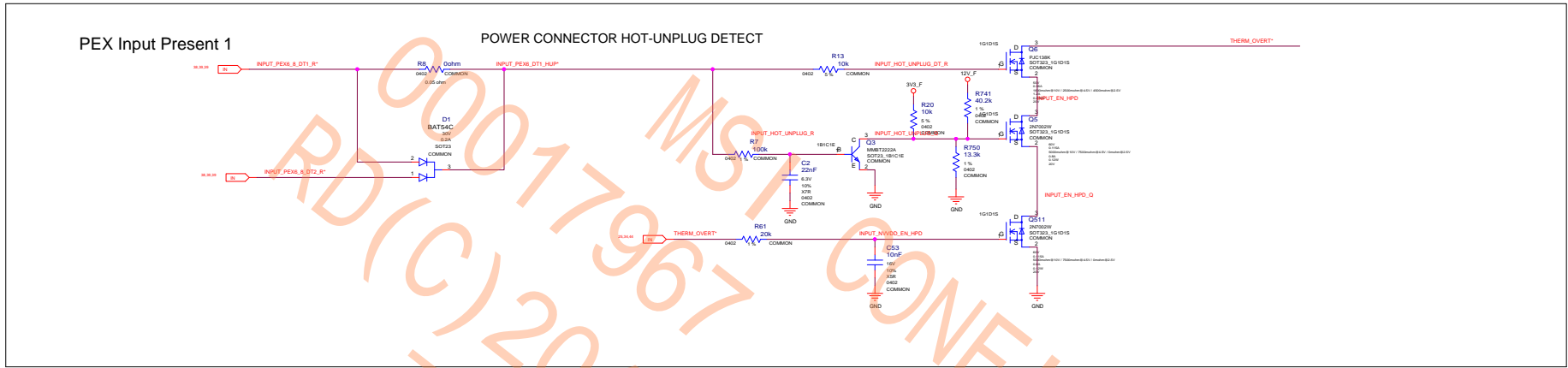
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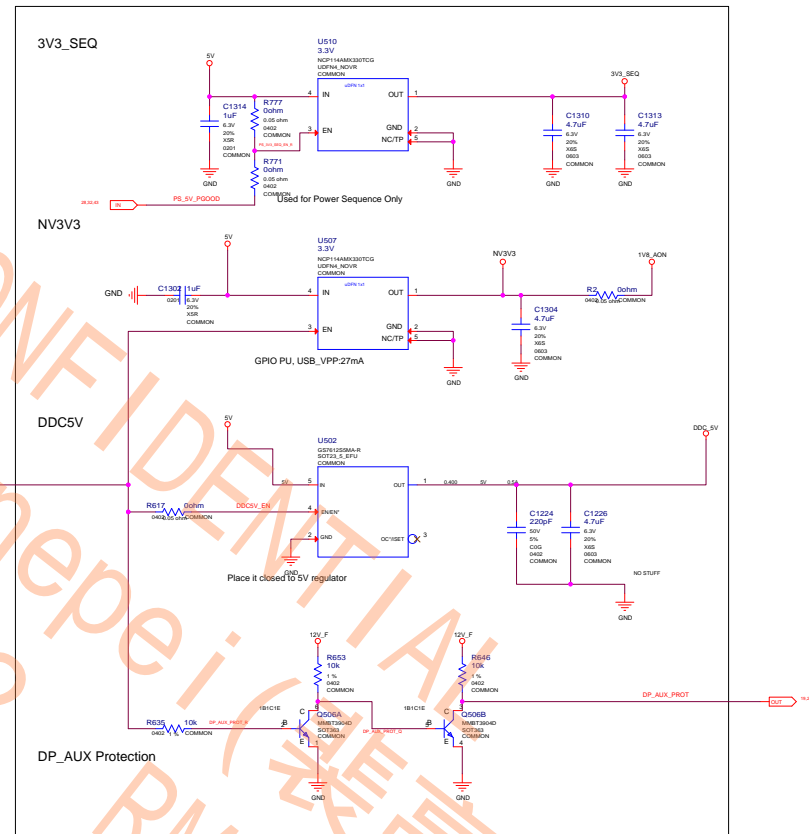
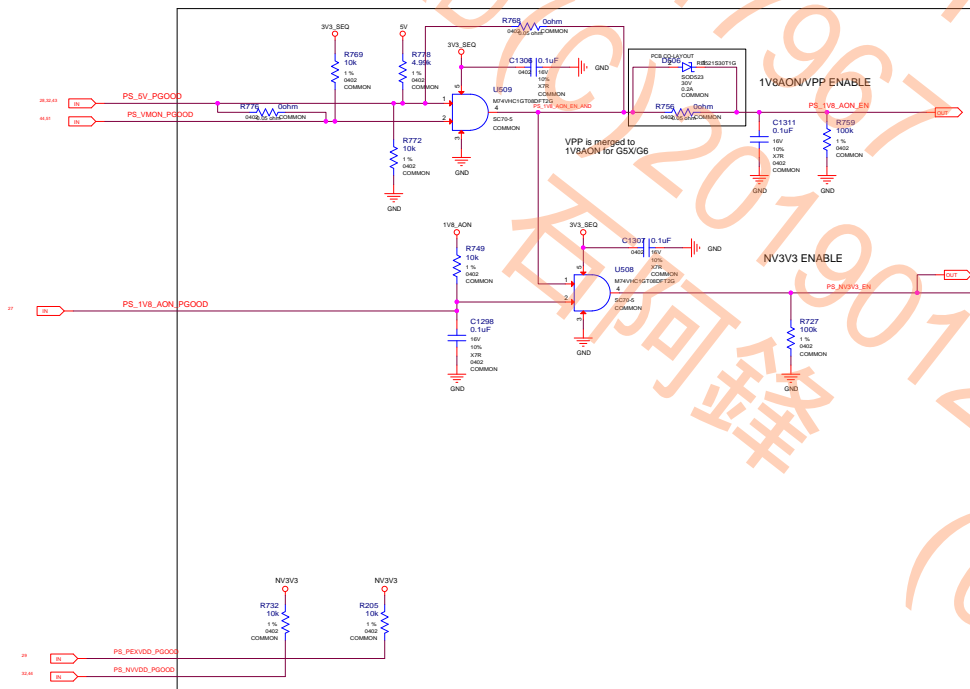
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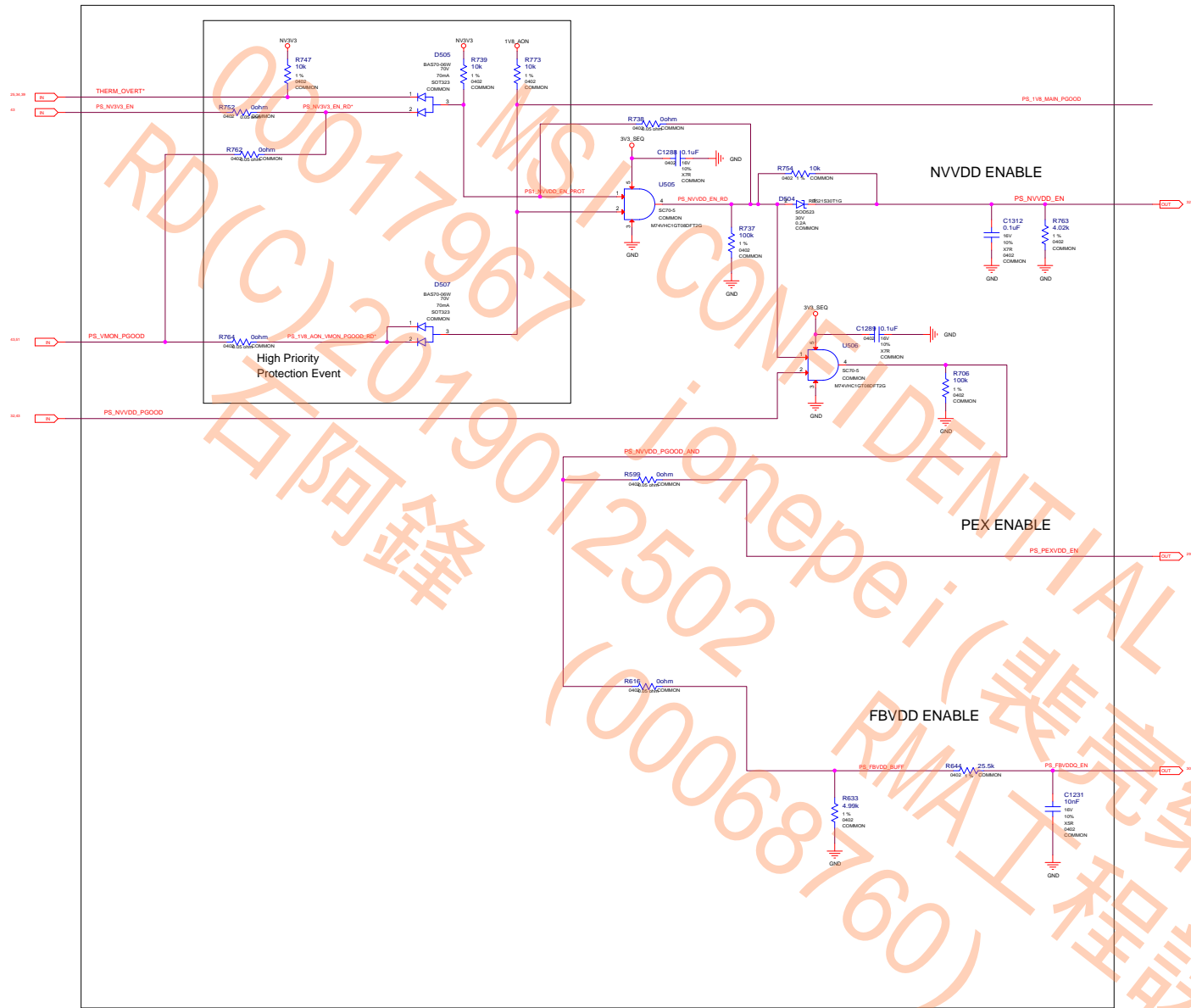
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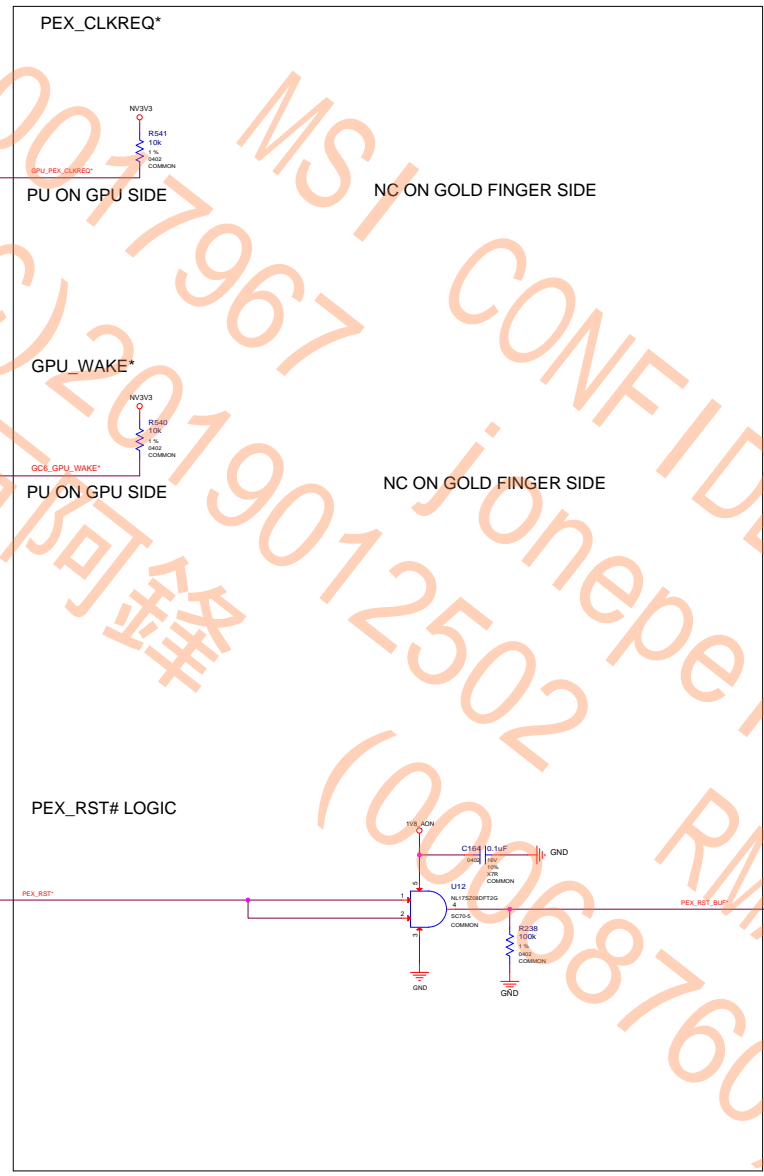
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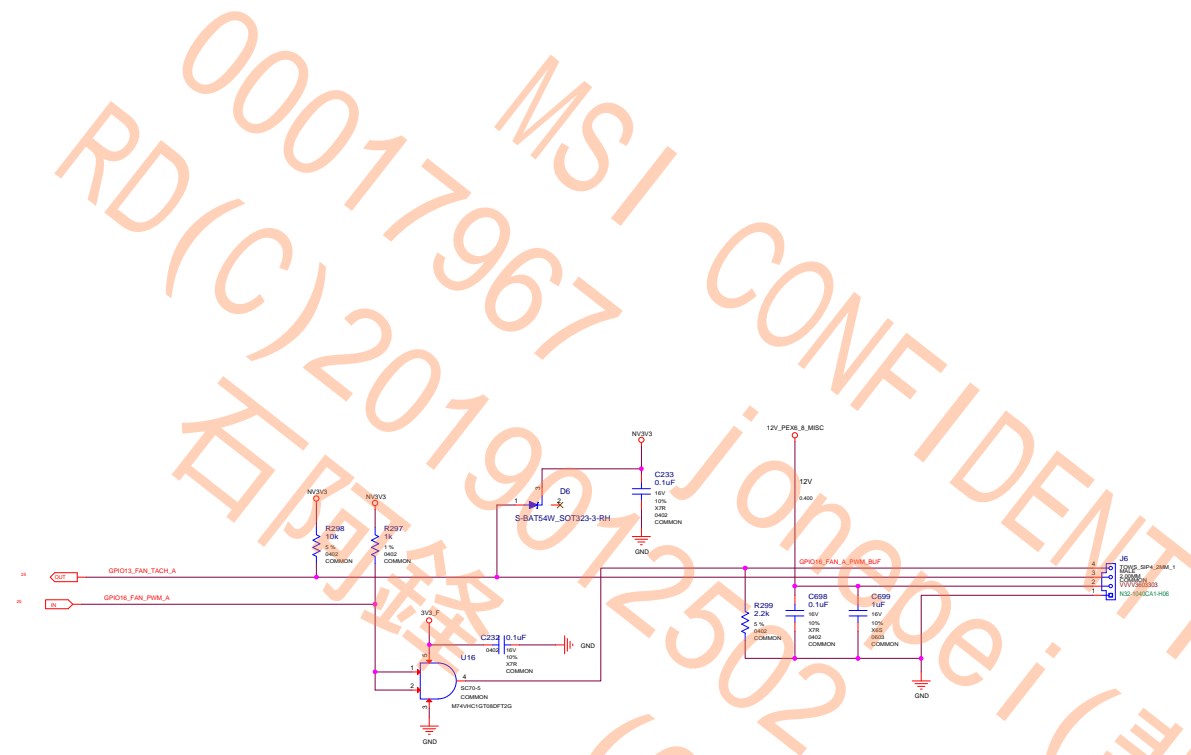
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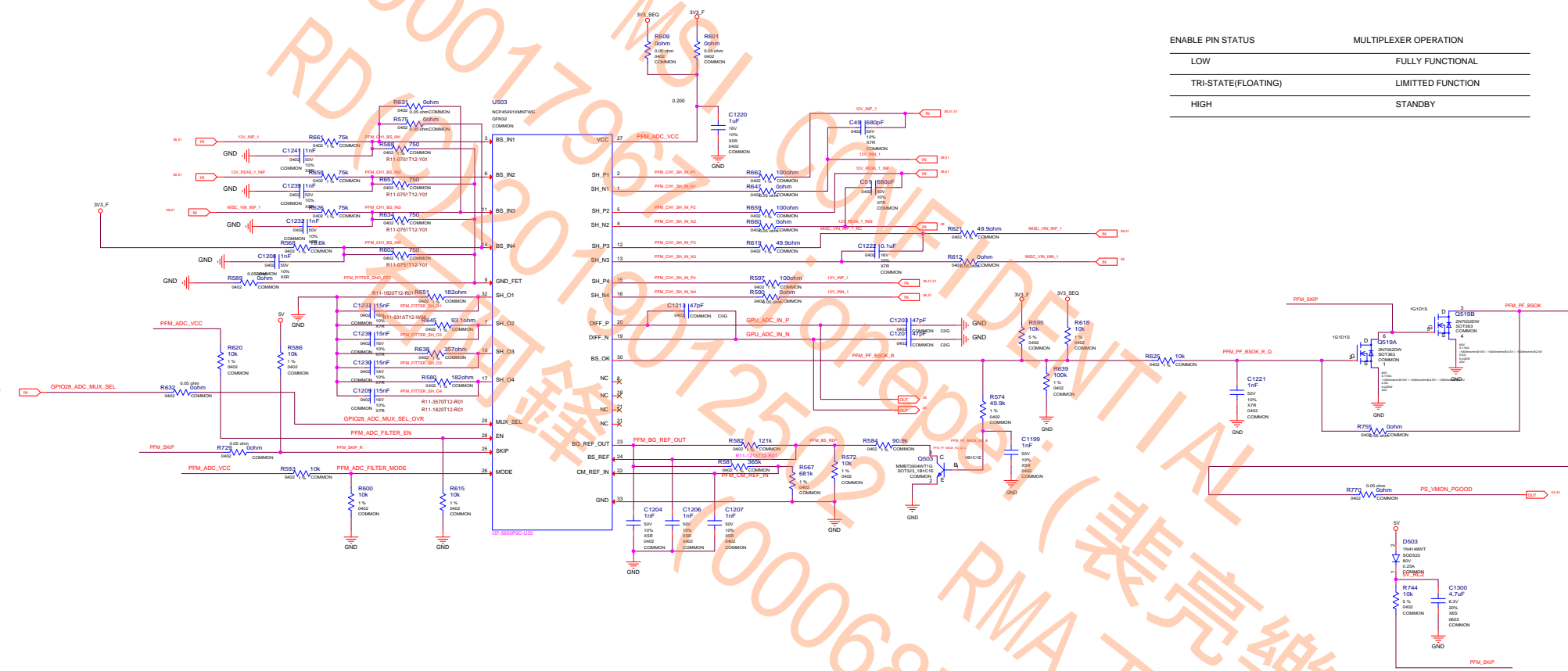
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MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



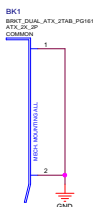
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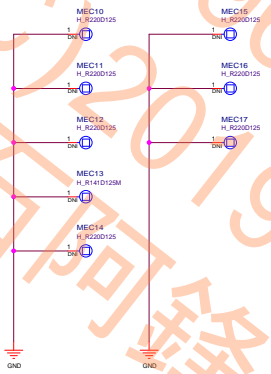
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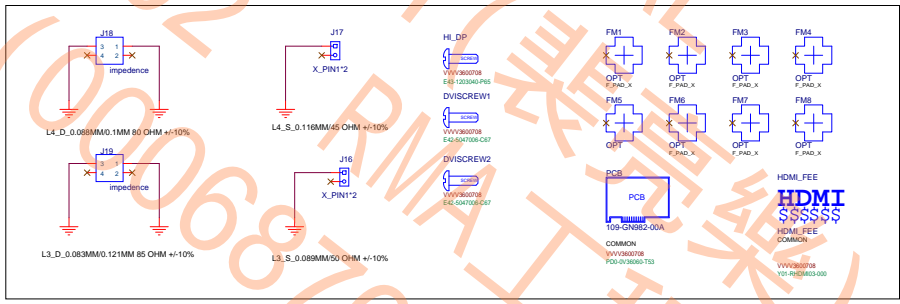
Bracket:



Mechanical Holes Symbol




BACK STIFFENER:



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