A CONTINUOUS MODEL FOR THE TAPPED-INDUCTOR BOOST CONVERTER

R. D. Middlebrook

California Institute of Technology
Pasadena, California 91125

ABSTRACT

A continuous, low-frequency, small-signal averaged model for the tapped-inductor boost converter with input filter is developed and experimentally verified, from which the dc transfer function and the small-signal line input and duty ratio input describing functions can easily be derived. A new effect due to storage-time modulation in the transistor switch is shown to explain observed excess filter damping resistance without associated loss in conversion efficiency. The presence of an input filter can cause a severe disturbance, even a null, in the control duty ratio describing function, with consequent potential performance difficulties in a converter regulator.

1. INTRODUCTION

A method of modeling switching converter transfer functions has been described by Wester and Middlebrook [1], and applied to the basic buck, boost, and buck-boost converters in the continuous conduction mode. The principle is to replace the several different, lumped, linear models that apply in successive phases of the switching cycle by a single lumped, linear model whose element values are appropriate averages over a complete cycle of their successive values within the cycle. The resulting "averaged" model permits both the input-to-output ("line") and duty ratio-to-output ("control") transfer functions to be easily obtained for both dc (steady state) and superimposed ac (describing function) inputs. The nature of the model derivation inherently restricts the validity to frequencies below the switching frequency, and model linearity is ensured by independent restriction of the superimposed ac signal to small amplitudes. The result is therefore a small-signal, low-frequency, averaged model.

The models obtained in [1] show that the line and control describing functions contain the anticipated low-pass LC filter response characterized by a pair of left half-plane poles and, if there is nonzero resistance in series with the capacitor, by a left half-plane real zero. The pole-pair positions are conveniently identified in terms of the filter corner frequency and peaking factor, or Q-factor. Two results of particular significance for the boost and buck-boost converters are that the filter corner frequency and Q-factor both vary with steady-state duty ratio D and, even more important, that the control describing function acquires a right half-plane real zero.

Several extensions and developments of the results of [1] are presented in this paper.

1. A small-signal, low-frequency, averaged model is derived for the tapped-inductor converter, of which the original ("simple") boost converter is a special case.

At the same time, the circuit being modeled is extended to include the line input filter that is almost invariably present in a practical system, and the modeling process is refined to include a more accurate representation of the circuit losses that affect the Q-factor. The motivation for the modeling refinement was to explain measured Q-factors that were significantly lower than predicted by the original model even when the most generous values for the physical loss-resistances were allowed. However, although the refined model did indeed predict lower Q-factors, the quantitative effect was still insufficient to explain the observed discrepancies.

It turned out that a quite different effect was responsible for the lower Q-factor, namely, modulation of the storage time of the transistor switch. The physical cause-and-effect sequence is as follows: an applied small-signal ac modulation of the switch duty ratio causes a corresponding modulation of the current carried by the switch at the instant of turn-off, and a consequent modulation of the storage time. The result is that the actual switch output duty ratio modulation amplitude is different from the switch drive modulation amplitude. It may seem surprising at first sight that this effect would cause only a lowering of the Q-factor, without affecting any of the other qualitative or quantitative features of the model;

nevertheless, this is indeed confirmed by the other principal extension presented in this paper:

2. A storage-time modulation effect in the switch is shown to result in an effective series resistance in the small-signal, low-frequency, averaged model of the tapped-inductor boost converter, whose presence lowers the apparent Q-factor of the low-pass filter characteristic contained in both the line and control describing functions.

Experimental results are presented for various conditions chosen specifically to expose the functional dependence of the model element values upon the several parameters, in order to maximize the degree of model verification thereby obtained. In addition to such quantitative verification, the following general conclusions are of particular interest:

1. The effective series resistance R_M in the model due to transistor switch storage-time modulation lowers the filter Q-factor, but it does not lower the conversion efficiency; in other words it is only an apparent resistance and not an actual loss resistance.

2. The presence of an LC input filter can cause a serious modification of the control describing function. A dip in the magnitude of the control describing function can occur in the neighborhood of the resonant frequency of the input LC filter. This dip is characterized by a complex pair of zeros in the control describing function. As the steady-state duty ratio is increased, as happens in normal regulation adjustment of a closed-loop converter system, the complex pair of zeros can not only reach the imaginary axis of the complex frequency plane, causing the dip in the magnitude response to become a null, but can move into the right half-plane causing a large amount of additional phase lag. A possible null in the control describing function magnitude response of course could severely degrade the performance, and the excessive phase lag could seriously affect the stability, of a closed-loop regulator system. The model presented here is useful in both the qualitative and quantitative design of such a system to guard against such disastrous eventualities.

2. DEVELOPMENT OF THE CONTINUOUS MODEL

The elements of a tapped-inductor boost converter are shown in Fig. 1. An input filter, which would invariably be used in a practical system, is included between the supply voltage V_g and the input of the converter itself. As far as the operation of the converter is concerned, only the filter elements L_s, R_s, and C_s need be explicitly represented; the box around the L_s is to imply that additional input filter elements may be present without affecting the nature of the converter operation. The resistances R_s and R_c in Fig. 1 are always present in a practical circuit even if they represent only capacitance esr.

Some waveforms in the circuit of Fig. 1 under steady state operation are shown in Fig. 2. The transistor switch is closed for a fraction

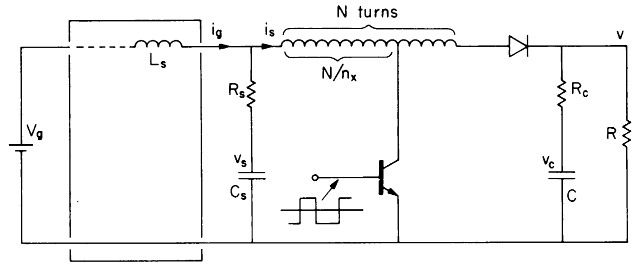

Fig. 1. Circuit of the tapped-inductor boost converter with input filter.

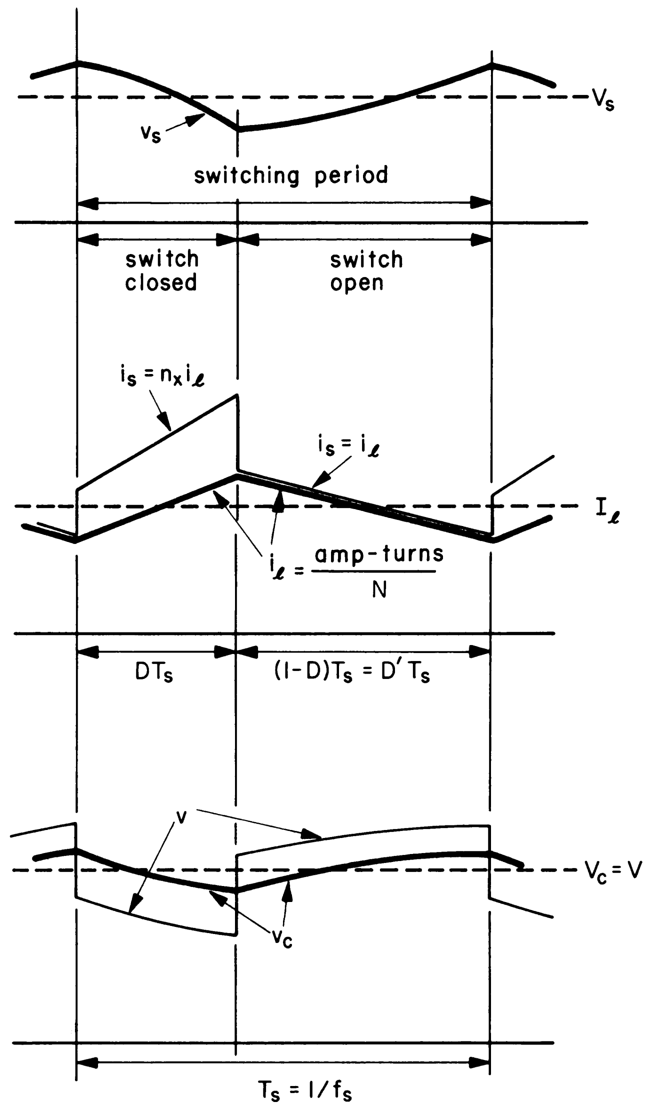

Fig. 2. Some waveforms in the circuit of Fig. 1: v_s, i_ℓ, and v_c are continuous; v is quasi-continuous; i_s is discontinuous.

T_sD of its period $T_s = 1/f_s$, where f_s is the switching frequency, and is open for the remaining fraction $T_sD' = T_s(1-D)$. While the switch is closed, the current i_s in the fraction N/n_x of the total inductor turns N ramps up as energy is stored in the inductor; part of i_s is supplied from the input by i_g, and the balance comes from discharge of C_s causing a fall in the capacitance voltage v_s. At the same time, the diode is open and the capacitance C discharges into the load R causing a fall in the voltage v_c. While the switch is open, the diode is closed and the current i_s in the total inductor turns N ramps down as the stored inductor energy discharges into the load and recharges C, causing a rise in v_c. Since i_s drops below i_g, C_s is recharged causing a rise in the voltage v_s.

Boundary conditions linking the waveforms in the two intervals depend upon the requirements that capacitance voltages and inductor ampere-turns cannot change instantaneously at the switching instants. Consequently, the voltages v_s and v_c are continuous at the switching instants, whereas the output voltage v has steps at the switching instants because of the drop in R_c. Similarly, the inductor ampere-turns is continuous at the switching instants, and it is convenient to illustrate this in terms of a quantity i_ℓ defined as "ampere-turns per turn," also shown in Fig. 2. Thus, i_ℓ is continuous but the actual inductor current i_s has steps of ratio n_x at the switching instants. Identification of i_ℓ is an important step in the derivation of the continuous model.

Waveforms shown in Fig. 2 are for the "continuous conduction" mode of operation in which the instantaneous inductor current does not fall to zero at any point in the cycle, and the entire discussion and results of this paper apply only to this mode. Average, or dc, values of the waveforms are also shown in Fig. 2. The dc output voltage V is of course equal to the dc voltage V_c on capacitance C.

A suitable equivalent of the circuit of Fig. 1 from which to begin derivation of the averaged model is shown in Fig. 3, and includes

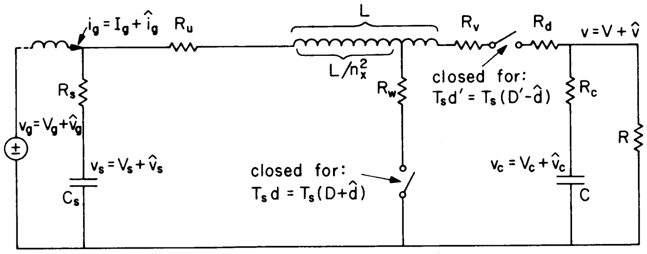

Fig. 3. Switched model equivalent to the circuit of Fig. 1; starting point for derivation of the continuous model of Fig. 10.

several parasitic resistances of obvious physical origin which are important in determining the effective Q of the implicit filter response characteristic. There are two independent "driving" signals: the line voltage v_g and the duty ratio d. Each is taken to have a dc part and small-signal ac part, so that $v_g = V_g + \hat{v}_g$ and $d = D + \hat{d}$. Since the "complementary" duty ratio 1-d frequently occurs in the equations, it is given the symbol $d' = 1-d$, so that $d' = 1-D-\hat{d} = D'-\hat{d}$. As a consequence of the dc and ac components of the two driving signals, all other voltages and currents in the circuit also have dc and ac components, in particular the output voltage $v = V + \hat{v}$. The analysis objective is to find a <u>continuous</u> model (unlike the switched model of Fig. 3) from which the dc and ac components of the output voltage V and $\hat{v}$ can be found from the dc and ac components of the two driving signals V_g, $\hat{v}_g$ and D, $\hat{d}$.

The approach taken is an extension of that in [1], in which the small-signal ac components $\hat{v}_g$, $\hat{d}$, etc. are taken to be slow compared with the switching frequency f_s. This restriction permits the nonlinear model of Fig. 3, which consists of two switched linear models, to be approximated by a linear model whose element values are appropriate averages of their values in the two intervals T_sd and T_sd'. Furthermore, this approach permits most of the analysis to be performed through successive transformations and reductions of circuit models; physical insight is thus better retained, and understanding made easier, than if analysis is performed entirely by algebraic manipulation. The result of this approach is an "averaged" model from which the two transmission characteristics can be obtained for dc and for ac at frequencies below the switching frequency.

The objective is to combine the two separate linear models of the piecewise-linear model of Fig. 3 into a single linear model. The procedure consists of a number of steps in manipulation of the model, which will be presented here for a slightly simplified version of Fig. 3 in which R_s, R_w, R_v, R_d, and R_c are set equal to zero. This is done so that the method may be illustrated without the burden of extra elements and terms which merely complicate the diagrams and equations. The effects due to these temporarily discarded elements will, however, be restored into the final results. Also, a number of comments concerned with the significance and interpretation of certain steps will be deferred until the end of the derivation.

<u>Step 1</u>. Draw separately the linear models of Fig. 3 that apply during each of the intervals T_sd, T_sd' as shown in Figs. 4(a) and 4(b) respectively. Identify the voltages and currents that are continuous across the switching instants, namely the capacitance voltages v_s, v_c, and the ampere-turns per turn of both the switched inductor, i_ℓ, and the input filter inductor, i_g.

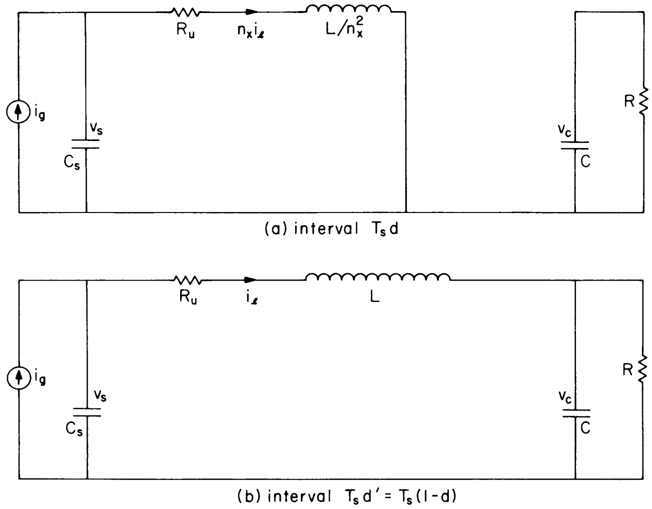

Fig. 4. Step 1 in the model derivation (parasitic resistances in model of Fig. 3 omitted): separate linear models that apply during the two intervals $T_s d$ and $T_s d'$.

Step 2. Manipulate the models of Fig. 4 to have both the same topology and the same values of the continuous voltages and currents at corresponding points, as shown in Fig. 5. In the present case, this requires scaling of the current $n_x i_\ell$ in Fig. 4(a) to match the current i_ℓ in Fig. 4(b), which is done by introduction of an ideal transformer of ratio $1:n_x$ in Fig. 5(a); since the voltage v_s is already the same in both models, the transformer is introduced to the right of C_s. To produce the same topology, a 1:1 transformer is introduced in the same place in Fig. 5(b). Also, since the current i_ℓ flows into C during interval $T_s d'$ but does not during interval $T_s d$, introduction of another ideal transformer to the left of C allows this condition to be realized with the same topology if the ratio is 0:1 in Fig. 5(a) and 1:1 in Fig. 5(b).

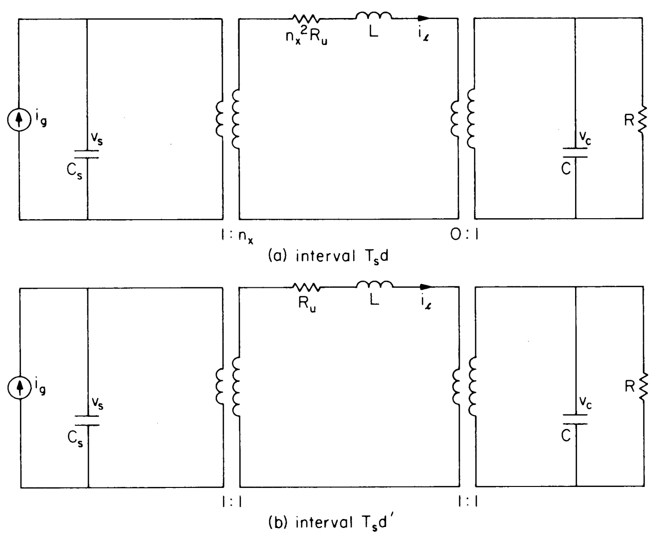

Fig. 5. Step 2: introduction of ideal transformers to establish the same topology and to expose the same continuous variables for the two intervals.

Step 3. Replace the ideal transformers in Fig. 5 by ideal dependent generators whose controlling signals are voltages or currents that are continuous across the switching instants. This is done in Fig. 6. (Notation: squares are used to represent dependent generators, circles represent independent generators.)

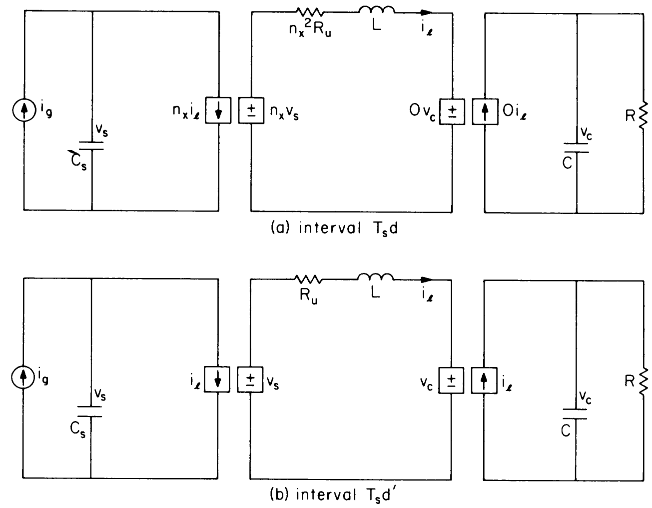

Fig. 6. Step 3: replacement of ideal transformer by dependent generators controlled by continuous variables.

Step 4. Coalesce the two topologically identical models of Figs. 6(a) and 6(b) into a single model in which the various signals have the average of their values throughout the entire period T_s, as shown in Fig. 7. For

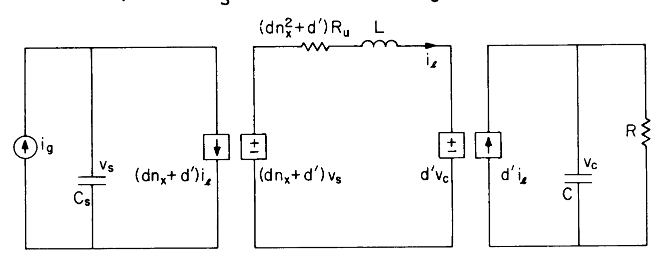

Fig. 7. Step 4: coalesced models for the two intervals into a single averaged model; implies imposition of the low-frequency restriction.

example, the dependent current generator which has a value $n_x i_\ell$ for an interval $T_s d$ and a value i_ℓ for an interval $T_s d'$ has an average value $(dn_x+d')i_\ell$ over the entire period T_s, and similarly for the other dependent generators. The pair on the right, of course, constitutes a special case in which the signal is zero for one of the intervals. The coalescing process takes a slightly different form for an element whose value is not the same in the two intervals: the resistance $(dn_x^2+d')R_u$ in Fig. 7 is the value having a voltage drop across it equal to the average of the voltage drops in the two intervals $T_s d$ and $T_s d'$.

Step 5. Substitute dc and ac components for the variables in Fig. 7. For example, the left-hand dependent current generator is expressed as:

$$(dn_x+d')i_\ell = [(D+\hat{d})n_x+(D'-\hat{d})](I_\ell+\hat{i}_\ell)$$

$$= (Dn_x+D')(I_\ell+\hat{i}_\ell)+(n_x-1)I_\ell\hat{d}+(n_x-1)\hat{i}_\ell\hat{d}$$

$$\approx (Dn_x+D')i_\ell+(n_x-1)I_\ell\hat{d}$$

The approximation of the final line is neglect of the ac product term, which is valid for small ac signals superimposed on the dc. This generator, therefore, may be decomposed into a dependent generator proportional to i_ℓ, and an independent generator proportional to the driving signal $\hat{d}$, as shown in Fig. 8. This figure shows

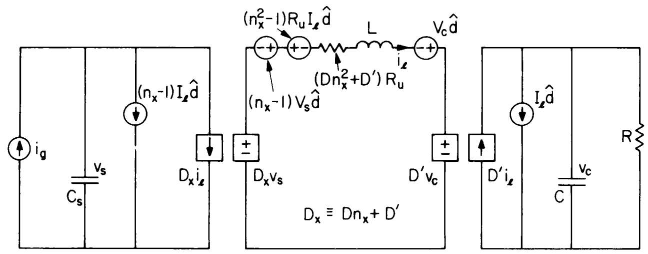

Fig. 8. Step 5: substitution of dc and ac components; implies imposition of the small-signal restriction.

corresponding manipulations of the other three dependent generators of Fig. 7. The substitution process for the averaged resistance is as follows. The voltage across $(dn_x^2+d')R_u$ is

$$(dn_x^2+d')R_ui_\ell = [(D+\hat{d})n_x^2+(D'-\hat{d})]R_u(I_\ell+\hat{i}_\ell)$$

$$\approx (Dn_x^2+D')R_ui_\ell+(n_x^2-1)R_uI_\ell\hat{d}$$

where again the product term in $\hat{i}_\ell\hat{d}$ is omitted. This voltage can be represented as that across a resistance plus an independent generator proportional to $\hat{d}$, as shown in Fig. 8. For conciseness, the factor Dn_x+D' is replaced by D_x.

Step 6. Replace the dependent generators by corresponding ideal transformers, and add a resistance R_u to the left of the D_x transformer, as shown in Fig. 9. To compensate for this addition, the reflected value $D_x^2R_u$ must be subtracted from the right-hand side of the D_x transformer so that the net resistance in this branch is then $[(Dn_x^2+D') - D_x^2]R_u$, which reduces to $DD'(n_x-1)^2R_u$ as shown in Fig. 9. One other change has been made in Fig. 9, namely the independent generator $I_\ell\hat{d}$ has been reflected from the right to the left side of the D' transformer.

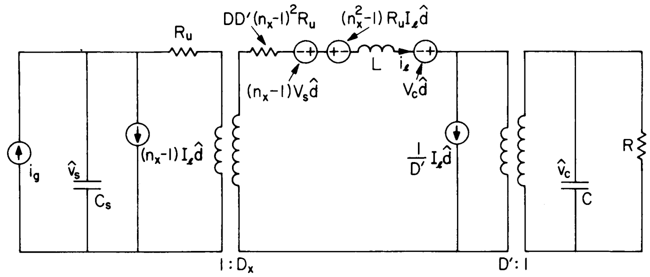

Fig. 9. Step 6: Restoration of ideal transformers in place of the dependent generators and adjustment of certain element positions.

As mentioned at the beginning of the derivation, the resistances R_s, R_w, R_v, R_d, and R_c were omitted. If these elements are included, the model of Fig. 9 becomes extended to that shown in Fig. 10, in which

$$\hat{e}_1 \equiv (n_x-1)V_s\hat{d} \qquad (1)$$

$$\hat{e}_2 \equiv V_c\hat{d} \qquad (2)$$

$$\hat{e}_3 \equiv [(D-D')(n_x-1)^2R_s - (n_x^2-1)R_u - (n_x^2R_w-R_v) - D'(R_c\| R)]I_\ell\hat{d} \qquad (3)$$

$$\hat{j}_1 \equiv (n_x-1)I_\ell\hat{d} \qquad (4)$$

$$\hat{j}_2 \equiv \frac{1}{D'}I_\ell\hat{d} \qquad (5)$$

$$R_1 \equiv DD'(n_x-1)[(n_x-1)(R_s+R_u)]+n_xR_w-R_v] \qquad (6)$$

$$R_2 \equiv DD'(R_d+R_c\|R) \qquad (7)$$

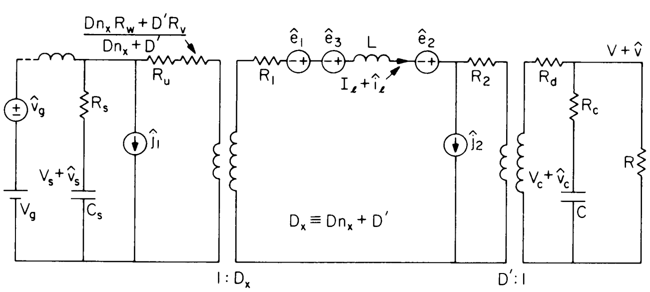

Fig. 10. Continuous, dc and low-frequency small-signal ac, averaged model for the tapped-inductor boost converter of Fig. 3 (parasitic resistances restored); D and $\hat{d}$ refer to duty ratio at the transistor collector.

The circuit of Fig. 10 is the complete continuous model of the tapped-inductor boost converter, including input filter, from which the dc and ac line and control transfer functions can easily be obtained.

The ideal transformers operate down to dc, and the dc output voltage V is obtained as a function of V_g and D by solution with the ac generators set equal to zero. Actually, to allow for an unspecified input filter, it is more convenient to solve for the dc output voltage V as a function of D and of the dc voltage at the input filter output, which is the same as the input filter capacitance voltage V_s. The dc component I_ℓ of the inductor ampere-turns per turn current is

$$I_\ell = \frac{D_x V_x}{D'^2 R + R_T} \qquad (8)$$

where

$$R_T \equiv D_x^2[R_u + (Dn_x R_w + D'R_v)/D_x] + R_1 + R_2 + D'^2 R_d \qquad (9)$$

is the total effective resistance referred to the middle loop in Fig. 10. The dc output voltage is then

$$V = D'I_\ell R = \frac{D_x}{D'} \frac{1}{1 + R_T/D'^2 R} V_s \qquad (10)$$

This equation represents the basic boost property of the converter; for a high-efficiency system, the effective dc loss resistance R_T is small compared with the reflected load resistance D'^2R, so $V \approx (D_x/D')V_s$. For reduction to the simple boost converter, $n_x = 1$ so $D_x = Dn_x + D' = 1$, and then $V \approx (1/D')V_s$.

The line describing function is obtained from the model of Fig. 10 by solution for $\hat{v}/\hat{v}_g$, and the control describing function is obtained as $\hat{v}/\hat{d}$ through use of the generators $\hat{e}_1$, $\hat{e}_2$, $\hat{e}_3$, $\hat{j}_1$, and $\hat{j}_2$, each of which is proportional to $\hat{d}$. Before consideration of such applications of the model, however, some comments will be made concerning its form and derivation.

The essence of the procedure of the model derivation is contained in step 4, in which the two models of Fig. 6 for the intervals $T_s d$ and $T_s d'$ are coalesced into a single model. The exact average of the two current generators, $n_x i_\ell$ from Fig. 6(a) and i_ℓ from Fig. 6(b), is $\langle dn_x i_\ell + d'i_\ell \rangle$. An essential approximation is then made in the replacement of the average of the product of two variables by the product of their averages, so that $\langle dn_x i_\ell + d'i_\ell \rangle = \langle dn_x i_\ell \rangle + \langle d'i_\ell \rangle \approx \langle d \rangle n_x \langle i_\ell \rangle + \langle d' \rangle \langle i_\ell \rangle = (\langle d \rangle n_x + \langle d' \rangle)\langle i_\ell \rangle$. It is this final form that is shown against the left-hand dependent current generator in Fig. 7, except that for simplicity in notation the averaging signs $\langle\rangle$ have been omitted. As described in [1], the above approximation is valid if at least one of the variables is continuous; in this case, d is not continuous (it changes from 1 to 0), but i_ℓ is continuous. As also discussed in [1], the averaging process imposes an upper frequency limit on the validity of the result, and it is for this reason that the model of Fig. 10 is a low-frequency averaged model, valid for ac signal frequencies much lower than the switching frequency.

The steps leading up to step 4 have the purpose not only of molding the separate linear models for the two switching intervals into similar topological forms, but also of setting up the quantities that are to be averaged in such a way that the current or voltage factor in the product is one that is continuous across the switching instants. Thus, in Figs. 6 and 7, the quantities to be averaged all contain i_ℓ, v_s, or v_C (actually, the state variables of the system) as one of the factors, and the inductor ampere-turns per turn i_ℓ was specifically identified for this purpose. In contrast, the actual inductor current i_s and the output voltage v, for example, are not continuous across the switching instants, as seen in Fig. 2, and their use is therefore suppressed in the manipulations leading up to step 4, although the details were not explicit because of omission of the various parasitic resistances.

In the final result of Fig. 10, all the parasitic resistances R_s, R_w, R_v, R_d, R_c, and also R_u which was retained throughout the derivation, appear in the same physical positions as in the original circuit of Fig. 3. (Although since R_w and R_v each appears in the original model for only one of the two switching intervals, they appear in Fig. 10 in an appropriately averaged form with an obvious physical interpretation. It is for this reason that these averaged forms are purposely inserted in the shown position in Fig. 10, just as R_u in the adjacent position was purposely added in step 6.)

In addition to the appearance of the parasitic resistances in the expected places, the model of Fig. 10 shows the presence of two additional resistances R_1 and R_2 defined by Eqs. (6) and (7), which are related to the parasitic resistances. It is interesting to note that R_1 and R_2 are zero at both zero and unity dc duty ratio (D = 0 and D' = 0), and have maximum values at D = D' = 0.5. The additional resistances R_1 and R_2 appear in the averaged model of Fig. 10 because of strict adherence in the derivation to the requirement that one of the two quantities in an averaged product must be continuous across the switching instant. However, as seen in the waveforms of Fig. 2, the output voltage v, for example, while not continuous may be considered quasi-continuous in that the steps are small compared to the total value. If quasi-continuity is accepted instead of strict continuity in step 4 of the derivation, then the resistances R_1 and R_2 do not appear in the result. This simplified procedure was followed in [1] in the derivation of an averaged model for the simple boost converter.

To see the significance of the "extra" resistances R_1 and R_2, consider the model of Fig. 10 reduced for determination of the line describing function $\hat{v}/\hat{v}_g$. For this case of constant duty ratio, the ê's and ĵ's are all zero, and for further simplicity let the input filter be omitted. Then, with the two transformers eliminated by appropriate reflection of the elements in the outer loops into the center loop, the resulting reduced model is as shown in Fig. 11. The line describing function $\hat{v}/\hat{v}_g$ is simply that of a lossy LC

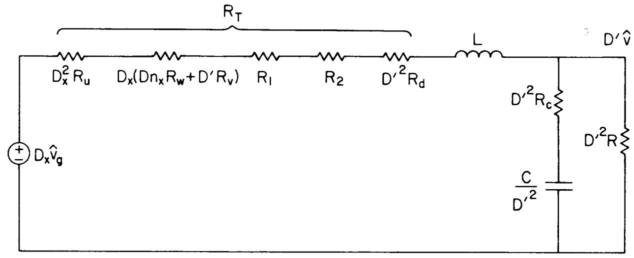

Fig. 11. Reduced version of averaged model of Fig. 10 for determination of the line describing function $\hat{v}/\hat{v}_g$, without input filter; R_T is the total effective series resistance.

filter whose Q-factor is determined (in part) by the total effective series resistance R_T, defined in Eq. (9) and in Fig. 11 as the sum of the various parasitic resistance elements shown. Clearly, R_1 and R_2 increase the effective loss and lower the Q.

The original motivation for the model derivation including strict continuity of one of the variables in an averaged product, which leads to the appearance of R_1 and R_2, was to explain measured Q factors in both the line and control describing functions that were significantly smaller than those predicted in the absence of R_1 and R_2. However, although the improved model provided a qualitative change in the right direction, the quantitative lowering of the Q caused by the addition R_1 and R_2 was insufficient to explain the observed results. An entirely different effect, discussed in the next section, was found to be the cause of the observed low Q.

3. MODEL EXTENSION FOR STORAGE TIME MODULATION EFFECT

When a measurement of the ac line describing function is made in the tapped-inductor boost converter shown in Fig. 1, an ac variation $\hat{v}_g$ is superimposed on the line voltage V_g and the transistor switch is driven from a modulator in such a way that the base drive is turned on and off with constant (dc) duty ratio, without any control signal ac modulation. As described above, such measurements showed a Q-factor significantly lower than could be accounted for by reasonable values of known parasitic loss resistance.

However, in the course of such measurements, it was noted that the transistor switch duty ratio at the collector was in fact being modulated by the injected line ac signal, in spite of the constant duty ratio base drive. Since the transistor collector turn-off is delayed after the base turn-off drive by the storage time, a possible explanation of the effect is that the storage time is being modulated by the line ac signal. This could occur because the line ac signal modulates the current carried by the transistor during the on-time, and the storage time is dependent upon the collector current to be turned off.

In an attempt to establish a quantitative model of this effect, an obvious starting point is an expression for storage time t_s as a function of the collector current I_C to be turned off, and of the base drive conditions. From well-known charge-control considerations, such an expression is [2]

$$t_s = \tau_s \ln\left[\frac{I_{B2} + I_{B1}}{I_{B2} + I_C/\beta}\right] \tag{11}$$

in which τ_s is the base carrier lifetime in the saturated "on" condition, I_{B1} is the forward base current just before turn-off, I_{B2} is the turn-off (reverse) base drive, and β is the active current gain for the collector current I_C at the end of the storage time. For typical turn-off overdrive such that $I_{B2} >> I_C/\beta$, the log may be expanded to give

$$t_s \approx t_{so} - \frac{\tau_s}{\beta I_{B2}} I_C \tag{12}$$

where

$$t_{so} \equiv \tau_s \ln(1 + I_{B1}/I_{B2}) \tag{13}$$

Hence, for constant base turn-on and turn-off drive currents, the storage time decreases linearly with increasing I_c to be turned off.

The next step is to incorporate this result into the duty ratio relationship. If the base is driven with duty ratio d_B so that the on-drive is present for an interval $T_s d_B$ of the switching period T_s, then the collector will remain "on" for an interval $T_s d$ given by

$$T_s d = T_s d_B + t_s \tag{14}$$

so that

$$d = d_B + \frac{t_{so}}{T_s} - \frac{I_C}{I_M} \tag{15}$$

where

$$I_M \equiv \frac{\beta I_{B2} T_s}{\tau_s} \tag{16}$$

is a "modulation parameter" that describes how the collector duty ratio d in Eq. (15) is affected by the collector current I_C.

In the context of the tapped-inductor boost converter of Fig. 1, the collector current to be turned off is the inductor current in the interval $T_s d$, namely $i_s = n_x i_\ell$ (Fig. 2). In general, the base drive duty ratio d_B has dc and small-signal ac components $d_B = D_B + \hat{d}_B$ that contribute to the corresponding components $i_\ell = I_\ell + \hat{i}_\ell$, so that, from Eq. (15),

$$d = \left(D_B + \frac{t_{so}}{T_s} - \frac{n_x I_\ell}{I_M}\right) + \left(\hat{d}_B - \frac{n_x}{I_M}\hat{i}_\ell\right) \qquad (17)$$

The dc and small-signal ac terms in the above equation represent respectively the dc and small-signal ac collector duty ratios D and $\hat{d}$ that were employed in the development of the continuous model of Fig. 10. All that is necessary, therefore, to account for the collector storage time modulation effect is to substitute the above expressions wherever D and $\hat{d}$ occur in the model of Fig. 10 and the associated equations (1) through (7). The dc substitution represents merely a small offset in the dc duty ratio, and is of no qualitative concern. In the ac substitution, the term of importance is that in $\hat{i}_\ell$, so that the five $\hat{e}$ and $\hat{j}$ generators of Fig. 10 and Eqs. (1) through (5) each gains an additional generator as shown explicitly in Fig. 12, in which

$$R_{M1} \equiv n_x(n_x-1)V_s/I_M \qquad (18)$$

$$R_{M2} \equiv n_x V_c/I_M \qquad (19)$$

$$R_{M3} \equiv n_x[(D-D')(n_x-1)^2R_s-(n_x^2-1)R_u - (n_x^2R_w-R_v) - D'(R_c\|R)]I_\ell/I_M \qquad (20)$$

$$K_1 \equiv n_x(n_x-1)I_\ell/I_M \qquad (21)$$

$$K_2 \equiv \frac{n_x}{D'} I_\ell/I_M \qquad (22)$$

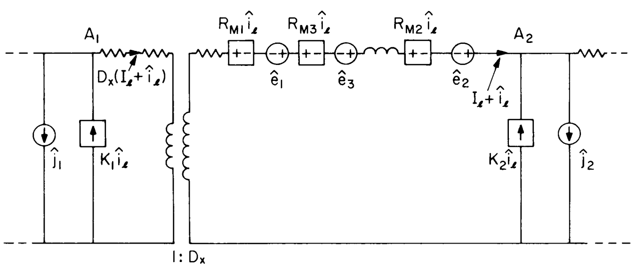

Fig. 12. Extension of model of Fig. 10 to include generators that represent the transistor storage-time modulation effect.

In Fig. 12, the $\hat{e}$ and $\hat{j}$ generators are still given by Eqs. (1) through (5), with $\hat{d}_B$ substituted for $\hat{d}$. However, now that the collector storage modulation effect has been explicitly accounted for in the model, it is more convenient merely to drop the sub B and to redefine D and $\hat{d}$ to refer to the base drive duty ratio rather than to the collector duty ratio, so that the small difference between D and D_B is implicitly ignored and Eqs. (1) through (5) remain applicable as they stand.

Some further manipulation of Fig. 12 leads to a simpler and more useful model. First, it is noted from Eq. (17) that $n_x I_\ell/I_M$ represents the difference between the collector and base dc duty ratios due to the influence of the collector dc current $n_x I_\ell$ upon the storage time. For normal designs this difference will be sufficiently small that $n_x I_\ell/I_M \ll 1$. It then follows from Eqs. (21) and (22) that $K_1 \ll 1$ and $K_2 \ll 1$, except perhaps for extreme conditions where $n_x \gg 1$ (very low inductor tap ratio), or $D' \ll 1$ (approaching unity duty ratio D). In Fig. 12, the ac current $K_1\hat{i}_\ell$ is summed with the ac current $D_x\hat{i}_\ell$ at point A_1, and the current $K_2\hat{i}_\ell$ is summed with $\hat{i}_\ell$ at point A_2; therefore, to the extent that $K_1, K_2 \ll 1$ both the K_1 and the K_2 generators in Fig. 12 have negligible effect and can be omitted from the model.

Second, it is seen that each of the R_M dependent generators in Fig. 12 is proportional to the ac current flowing through it, and can therefore be directly replaced by the corresponding resistance.

The resulting model is shown in Fig. 13, in which the K_1 and K_2 generators are dropped and the $\hat{e}$ generators and R_M resistances are condensed to

$$\hat{e} = \hat{e}_1 + \hat{e}_2 + \hat{e}_3 \qquad (23)$$

$$R_M = R_{M1} + R_{M2} + R_{M3} \qquad (24)$$

Some reduction and simplification in these expressions can be achieved by comparison of the contributing terms. From Eq. (10), $V_c = V = D'I_\ell R$ and it can then be seen from Eqs. (2), (3) and (19), (20) that the ratios $\hat{e}_3/\hat{e}_2$ and R_{M3}/R_{M2} are on the order of the ratio between

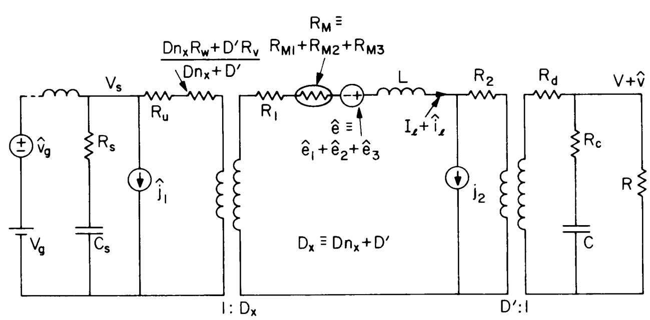

Fig. 13. Complete continuous, dc and low-frequency small-signal ac, averaged model for the tapped-inductor boost converter of Fig. 3, including the "modulation resistance" R_M which is present only in the ac model; D and $\hat{d}$ refer to duty ratio at the transistor base.

some combination of the parasitic resistances and the load resistance R; consequently, the contributions $\hat{e}_3$ and R_{M3} can be dropped in Eqs. (23) and (24). Then, from Eq. (10) with a similar degree of approximation, $V = (D_x/D')V_s$ and the remaining terms in Eqs. (23) and (24) can be combined to give

$$\hat{e} = \frac{n_x}{D_x} V\hat{d} \qquad (25)$$

$$R_m = \frac{n_x^2}{D_x} \frac{V}{I_M} = \frac{n_x^2}{D_x} \frac{\tau_s V}{\beta I_{B2} T_s} \qquad (26)$$

The final model is a continuous, averaged model for the tapped-inductor boost converter with input filter, including the transistor switch storage-time modulation effect accounted for by the resistance R_M. It is valid for both dc and small-signal ac with the proviso that the resistance R_M is to be included only in the ac model and not in the dc model. This is necessary because of the step by which the model of Fig. 13 was obtained from that of Fig. 12: the total current through the R_M generators of Fig. 12 is $I_\ell + \hat{i}_\ell$, but the generators are functions only of the ac component $\hat{i}_\ell$. In the final model of Fig. 13, the resistance R_M is enclosed in an oval as a reminder that it is to be included only in the ac model.

It is seen from Fig. 13 that inclusion of the storage-time modulation effect leads to a modification in the model that is at least potentially capable of explaining the observed properties: the appearance of the ac resistance R_M lowers the Q of the implicit filter characteristic, and the fact that the effect is represented only by a resistance confirms that no other property of the model is affected.

The storage-time modulation effect is manifested through two parameters: first, the parameter I_M defined in Eq. (16) is determined by transistor internal properties τ_s and β, and by the switch input circuit drive conditions described by the period T_s and the turn-off base current I_{B2}; second, the parameter R_M which, by Eqs. (18) through (20) and (23), is inversely proportional to I_M and is a function also of the switch output circuit, namely the boost converter element values and operating conditions.

4. MODEL REDUCTION AND EXPERIMENTAL VERIFICATION

Although the qualitative nature of the dc characteristic V as a function of V_g and D and of the ac line describing function $\hat{v}/\hat{v}_g$ are obvious from the model of Fig. 13, the nature of the ac control describing function $\hat{v}/\hat{d}$ is not so obvious because the driving signal enters through the three separate generators $\hat{e}$, $\hat{j}_1$, and $\hat{j}_2$. Understanding and interpretation of this characteristic is therefore facilitated by some further manipulation and reduction of the circuit of Fig. 13 for some special cases.

If the input filter is omitted, the $\hat{j}_1$ generator becomes mmaterial, and one step in reduction of the model of Fig. 13 for calculation of the control describing function may be accomplished as in Fig. 14, in which the

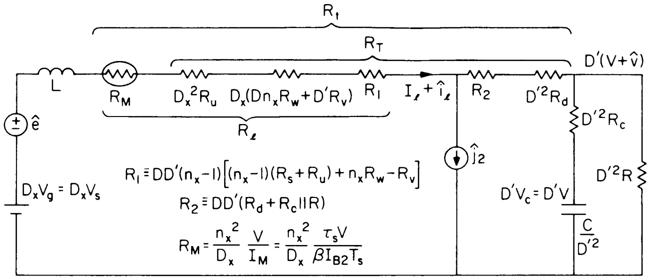

Fig. 14. Partially reduced version of averaged model of Fig. 13 for determination of the control describing function $\hat{v}/\hat{d}$, without input filter.

D_x and D' ideal transformers have been eliminated by reflection of the elements of the left and right loops into the center loop. The circuit of Fig.14 contains both the dc and ac models, and certain resistance combinations of interest are identified in the figure: R_ℓ is the ac resistance to the left of $\hat{j}_2$, R_T is the total effective dc series loss resistance, and R_t is the total effective ac series damping resistance. The distinction between R_t and R_T occurs because the storage-time modulation resistance R_M contributes to ac damping, but does not contribute to loss because it is absent in the dc model.

A final reduction of the model is made in Fig. 15, in which the two remaining independent

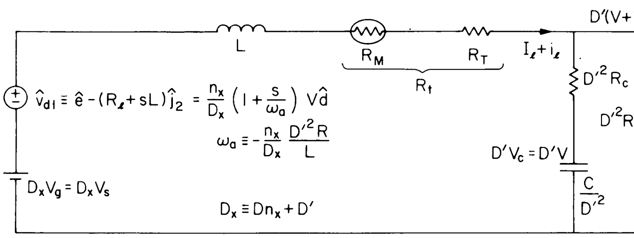

Fig. 15. Fully reduced version of model of Fig. 14, showing appearance of right half-plane zero ω_a; R_T is the total effective dc series loss resistance, and R_t is the total effective ac series damping resistance.

generators are combined into a single generator given by

$$\hat{v}_{d1} \equiv \hat{e} - (R_\ell + sL)\hat{j}_2 \qquad (27)$$

With substitution for $\hat{e}$ and $\hat{j}_2$ from Eqs. (25) and (5), together with the dc relation $V = D'I_\ell R$ from Eq. (10), Eq. (27) becomes

$$\hat{v}_{d1} = \left[\frac{n_x}{D_x} - (R_\ell + sL)\frac{1}{D'^2R}\right] V\hat{d} \qquad (28)$$

Again with neglect of the ratio of parasitic resistances to the reflected load resistance, the term in R_ℓ may be dropped so that

$$\frac{\hat{v}_{d1}}{V\hat{d}} = \frac{n_x}{D_x}\left(1 + \frac{s}{\omega_a}\right) \qquad (29)$$

which is also shown in Fig. 15, where

$$\omega_a \equiv -\frac{n_x}{D_x}\frac{D'^2 R}{L} \tag{30}$$

The response of the ac output voltage $\hat{v}$ to the effective driving voltage $\hat{v}_{d1}$ in Fig. 15 is simply that of the lossy low-pass filter. In terms of suitably normalized quantities, the result for the overall control describing function $\hat{v}/\hat{d}$ is

$$\frac{\hat{v}}{V\hat{d}} = \frac{n_x}{D_x}\frac{(1+s/\omega_z)(1+s/\omega_a)}{1+\frac{1}{Q'}\left(\frac{s}{\omega_o'}\right)+\left(\frac{s}{\omega_o'}\right)^2} \tag{31}$$

where

$$\frac{\omega_o'}{\omega_o} = D' \quad (32) \qquad \frac{\omega_z}{\omega_o} = Q_c \quad (33) \qquad \frac{\omega_a}{\omega_o} = -\frac{n_x}{D_x}D'^2 Q_L \quad (34)$$

$$\frac{1}{Q'} = \frac{1}{D'}\left[\frac{1}{Q_t}+\frac{1}{Q_L}+\frac{D'^2}{Q_c}\right] \tag{35}$$

and in which

$$\omega_o \equiv \frac{1}{\sqrt{LC}} \quad (36) \qquad Q_t \equiv \frac{\omega_o L}{R_t} \quad (37)$$

$$Q_c \equiv \frac{\omega_o L}{R_c} \quad (38) \qquad Q_L \equiv \frac{R}{\omega_o L} \quad (39)$$

are normalized parameters related to the original elements in Fig. 3. In the above results, terms in the ratio R_t/D'^2R have been neglected compared to unity.

Equation (31), referring to the model of Fig. 15, shows that, for the tapped-inductor boost converter of Fig. 1 without input filter, the control transmission frequency response is qualitatively the same as previously obtained for the simple boost converter in [1]. That is, the response is characterized by a low-pass filter whose corner frequency ω_o' and peaking factor Q' both change with dc duty ratio D, a zero ω_z due to R_c which is constant, and a negative zero ω_a which results from the switching action and which also changes with D. The pole-zero pattern in the s-plane is therefore as shown in Fig. 16, in which the pole pair and the zero ω_z are in the left half-plane and the zero ω_a is in the right half-plane. The arrows indicate motion with increasing D. It is interesting to note that ω_a is in the right half plane because of the subtraction of the contribution of the generator $\hat{j}_2$ from that of the generator $\hat{e}$ in the single generator $\hat{v}_{d1}$ in Fig. 15.

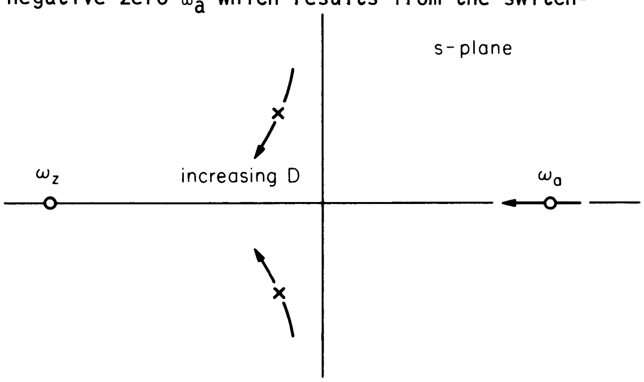

Fig. 16. Pole-zero pattern in the s-plane for the control describing function $\hat{v}/\hat{d}$ obtained from the model of Fig. 15.

Experimental verification of various aspects of the continuous model of Fig. 13 have been made. The first objective was to confirm aspects of the model related to the storage-time modulation resistance R_M. The circuit of Fig. 17 was constructed, which corresponds to that of Fig. 1 with the input filter omitted.

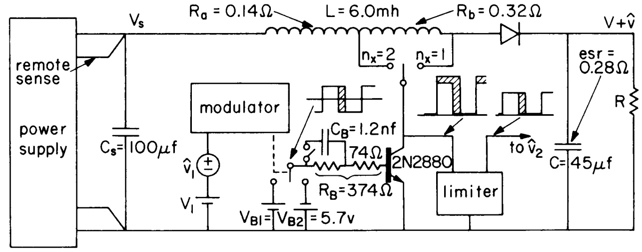

Fig. 17. Experimental tapped-inductor boost converter without input filter. Base drive duty ratio ac modulation is imposed by $\hat{v}_1$, and the resulting collector duty ratio ac modulation is monitored at $\hat{v}_2$.

In the circuit of Fig. 17, the inductor consisted of 100 turns of #20 wire of resistance $R_a = 0.14\Omega$ to the $n_x = 2$ tap, plus 100 turns of #24 wire of resistance $R_b = 0.32\Omega$ wound on an Arnold A930157-2 MPP $\mu = 125$ toroid. Independent measurements showed that the inductance at typical dc current levels was L = 6.0mh. The capacitor C was a combination of solid tantalums which independent measurements showed to have a capacitance C = 45μf and esr = 0.28Ω. The 2N2880 power transistor was switched through a base resistance R_B = 374Ω between voltages $+V_{B1}$ = +5.7v and $-V_{B2}$ = -5.7v by a modulator that provided fixed-frequency, trailing-edge modulation controlled by dc and small-signal ac input voltages V_1 and $\hat{v}_1$.

A preliminary experiment was done to measure the modulation parameter I_M determined by the switch transistor and its input circuit. Combination of Eqs. (12) and (16) shows that the "normalized" storage time is a linear function of I_C:

$$\frac{t_s}{T_s} = \frac{t_{so}}{T_s} - \frac{I_C}{I_M} \tag{40}$$

From the waveforms of Fig. 2, it is easily seen that I_C, which is the current in the transistor just before turn-off, is given by

$$I_C = n_x\left(I_\ell + \frac{V-V_s}{L}\,\frac{D'T_s}{2}\right) \qquad (41)$$

From Fig. 15, $V \approx (D_x/D')V_s$ and $I_\ell \approx (D_x/D'^2R)V_s$, so the above equation reduces to

$$I_C = \frac{n_x D_x V_s}{D'^2}\left(\frac{1}{R} + \frac{n_x DD'^2 T_s}{2D_x L}\right) \qquad (42)$$

Measurements of storage time t_s, taken directly from an oscilloscope, were made for various combinations of V_s, R and D in the circuit of Fig. 17 (without the speedup capacitor C_B) with switching frequency $f_s = 1/T_s = 10$kHz and $n_x = 1$ (simple boost converter configuration). Resulting data points of t_s/T_s vs. I_C from Eq. (42) are shown in Fig. 18, from which the measured slope gives $I_M = 40$ amps.

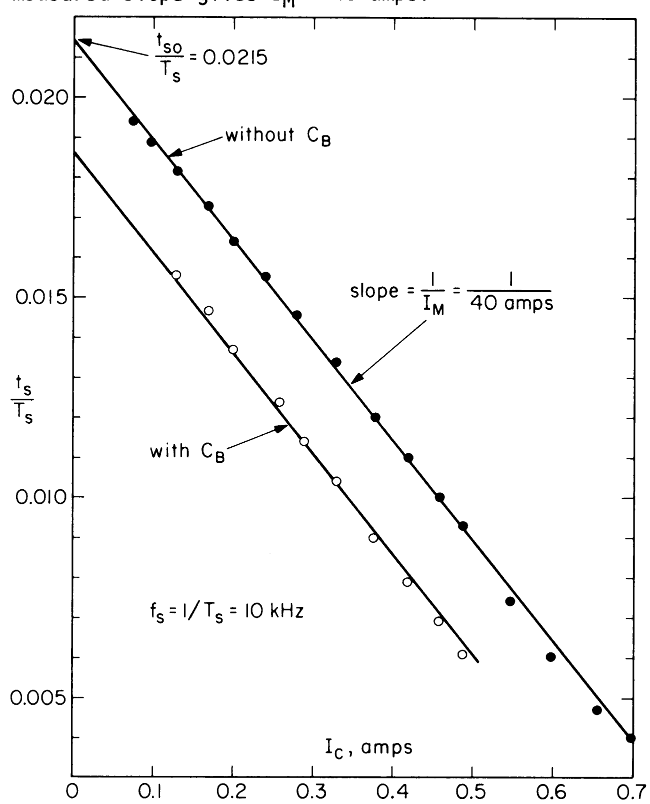

Fig. 18. Determination of the "modulation parameter" I_M by oscilloscope observation of the collector storage time t_s in the circuit of Fig. 17 ($n_x = 1$).

As a matter of interest, the transistor parameters τ_s and β may also be deduced from these results. From Fig. 18, the vertical axis intercept is $t_{so}/T_s = 0.0215$, so $t_{so} = 2.15\mu$sec. From Eq. (13), $\tau_s = t_{so}/\ln(1+I_{B1}/I_{B2})$ in which $I_{B1} = (V_{B1} - V_{BE})/R_B = 13$ma and $I_{B2} = (V_{B2} + V_{BE})/R_B = 17$ma, where $V_{BE} \approx 0.7$v is the forward base-emitter threshold voltage of the transistor, which leads to $\tau_s = 3.8\mu$sec. Then, from Eq. (16), $\beta = \tau_s I_M/I_{B2}T_s = 90$. Also as a matter of interest, data are also shown in Fig. 18 for base drive including the speedup capacitor $C_B = 0.0012\mu$f. As expected, this reduces the storage time but does not alter its rate of change with I_C, so that the modulation parameter I_M remains the same.

A group of measurements was then made for the purpose of exposing the effect of the storage-time modulation resistance R_M upon the effective damping of the filter characteristic in the control describing function. The circuit of Fig. 17 was used, reduced to the simple boost converter configuration with $n_x = 1$, so that $D_x = Dn_x + D' = 1$ for all D. A Hewlett-Packard 302A Wave Analyzer in the BFO mode was used as an oscillator and automatically tracking narrow-band voltmeter. The oscillator output provides the ac control signal $\hat{v}_1$, and the voltmeter reads the ac output voltage $\hat{v}$. There is no signal frequency dependence in the modulator, so that the ac duty ratio $\hat{d}$ at the modulator output is proportional to $\hat{v}_1$, independent of frequency. The measurements of the control describing function $\hat{v}/\hat{v}_1$ should therefore have a frequency response predicted by $\hat{v}/\hat{d}$ from the model of Fig. 15.

As will be seen, the larger part of the effective damping resistance R_t is the modulation resistance R_M; the effective loss resistance R_T is therefore inaccurately determined from R_t, and is also inaccurately determined by calculation from the various parasitic resistances since they themselves are not accurately known.

It happens that the effective loss resistance can be determined directly by a different measurement in the circuit of Fig. 17. As indicated, the transistor collector waveform, in the presence of $\hat{v}_1$, is modulated both in amplitude and duty ratio. If this waveform is put through a limiter, the output has constant amplitude and the same duty ratio modulation. If the limiter output is applied to the analyzer input, the analyzer narrow-band voltmeter gives a reading $\hat{v}_2$ proportional to the duty ratio modulation. Hence, $\hat{v}_2$ is proportional to the actual collector duty ratio modulation, which is different from the base drive duty ratio modulation becuase of the storage-time modulation effect, and so a measurement of $\hat{v}/\hat{v}_2$ in the circuit of Fig. 17 gives the control describing function that would exist if there were no storage-time modulation. The frequency response of this characteristic would therefore be predicted by the model of Fig. 15 with R_M absent, so that a direct measurement of R_T can be obtained.

A measurement of the characteristic $|\hat{v}/\hat{v}_2|$ made in this way on the circuit of Fig. 17 with $n_x = 1$ is shown as curve (a) in Fig. 19. The measurement conditions were $f_s = 20$kHz, D = 0.25, V = 50v, and R = 240Ω. From Eq. (36), the normalizing frequency is $f_o = \omega_o/2\pi = 310$Hz, and from Eq. (32) the effective filter corner frequency is $f_o' = D'f_o = 0.75 \times 310 = 230$Hz. As seen from curve (a) in Fig. 19, the measured

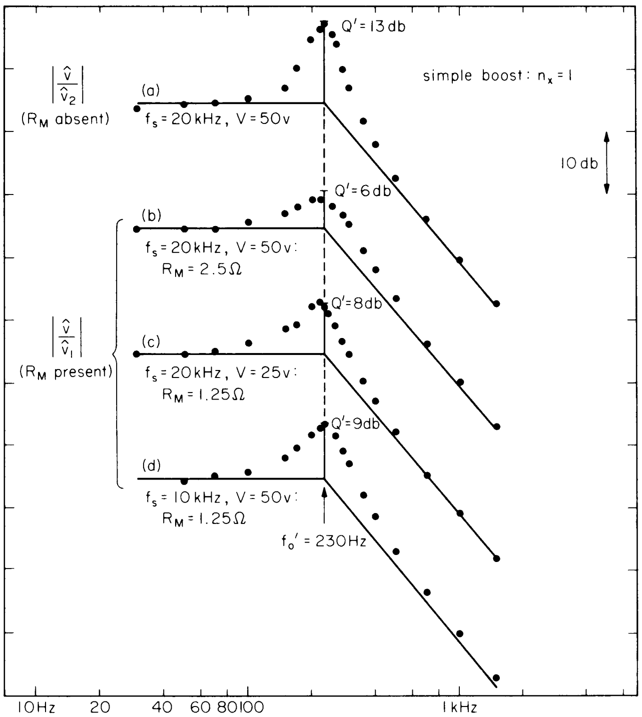

Fig. 19. Exposure of effect of modulation resistance R_M on the control describing function peaking factor Q' in the circuit of Fig. 17 with n_x = 1 and D = 0.25; (a) determination of R_T = 1.2Ω from observed Q' = 13db; (b), (c), (d) predicted lower Q' when various calculated values of R_M are included, and observed data points.

corner frequency is essentially equal to this predicted value. Curve (a) also indicates that the peaking factor is Q' = 13db → 4.47. From Eq. (35), the total effective damping is due to Q_t, Q_L, and Q_C; for the present case, from Eqs. (38) and (39), $Q_C = \omega_o L/R_C$ = 11.4/0.28 = 41 in which R_C = 0.28Ω is the capacitance esr, and $Q_L = R/\omega_o L$ = 240/11.4 = 21. Then, with use of the measured Q' = 4.47, Eq. (35) may be solved to give Q_t = 9.39. Finally, from Eq. (37) with R_t replaced by R_T because R_M is absent under the conditions of this measurement, $R_T = \omega_o L/Q_t$ = 1.2Ω. This is a reasonable value, since for n_x = 1 R_u is the total inductor resistance $R_u = R_a+R_b$ = 0.46Ω, which leaves 1.2 - 0.46 ≈ 0.7Ω for the remaining parasitic resistances.

With R_T thus directly determined from the response $\hat{v}/\hat{v}_2$, attention can be returned to the actual control describing function $\hat{v}/\hat{v}_1$ in which the modulation resistance R_M is present in the model of Fig. 15. Curve (b) in Fig. 19 shows $|\hat{v}/\hat{v}_1|$ for the circuit of Fig. 17 under the same conditions as for curve (a), namely f_s = 20kHz, D = 0.25, R = 240Ω. For n_x = 1, the expression given by Eq. (26) is $R_M = V/I_M = \tau_s V/\beta I_{B2} T_s$. As previously determined by independent measurement, I_M = 40 amps for f_s = 10kHz; therefore, since I_M is proportional to the switching period T_s, I_M = 20 amps under the condition f_s = 20kHz for curve (b) in Fig. 19, and then $R_M = V/I_M$ = 50/20 = 2.5Ω. With use of the value R_T = 1.2Ω already found, the total effective series damping resistance in the model of Fig. 15 is $R_t = R_M + R_T$ = 2.5 + 1.2 = 3.7Ω, which from Eq. (37) gives $Q_t = \omega_o L/R_t$ = 11.4/3.7 = 3.08. Then, from Eq. (35) with Q_L = 21, Q_C = 41, and D = 0.25, the total effective peaking factor is Q' = 1.94 → 6 db. The direct measurement of curve (b) shows a Q' of about 5db, so that the presence of the modulation resistance R_M = 2.5Ω in the model of Fig. 15 accounts both qualitatively and quantitatively for the considerable lowering of the peaking factor by about 8db.

Another result due to R_M is a change in effective filter peaking factor Q' with change of voltage operating level or of switching frequency, which would not occur in the absence of the storage-time modulation effect. In the simple boost converter with n_x = 1, $R_M = V/I_M = \tau_s V/\beta I_{B2} T_s$ and is therefore proportional to both V and $f_s = 1/T_s$. Curve (c) in Fig. 19 shows the control transmission characteristic under the same conditions as for curve (b) except that V_s is halved, which similarly scales all the dc values, including the output voltage V. Hence, for I_M = 20 amps, R_M is halved to 1.25Ω and R_T stays the same at 1.2Ω, so that R_t = 2.45Ω. With all other quantities the same, Q' = 2.90 → 9db which agrees well with the measured value of 8db in curve (c). Alternatively, if V is restored to 50v but the switching frequency is halved to f_s = 10kHz, I_M doubles to 40 amps and R_M = 1.25Ω again, so that Q' remains at 9db, which is the value measured in curve (d) in Fig. 19.

Attention is now turned to measurements under conditions that expose the right half-plane zero ω_a in the model of Fig. 15. Still for the simple boost converter configuration n_x = 1, measurements of the control describing function $\hat{v}/\hat{v}_1$ were taken on the circuit of Fig. 17 under the condition f_s = 20kHz, D = 0.6, V = 25v, and R = 162Ω. Data points of both magnitude and phase of $\hat{v}/\hat{v}_1$ are shown in Fig. 20. The phase measurements were also taken with the Hewlett-Packard 302A Wave Analyzer, by techniques that have been described elsewhere [3]. The control describing function predicted by the model of Fig. 15 is obtained as follows.

The normalizing frequency is f_o = 310Hz, and from Eq. (32) the effective filter corner frequency is $f_o' = D'f_o$ = 0.4 x 310 = 130Hz. From Eqs. (38) and (39), Q_C = 41 and Q_L = 14. At f_s = 20kHz, I_M = 20 amps and the corresponding modulation resistance is $R_M = V/I_M$ = 25/20 = 1.25Ω. With the parasitic loss resistance still R_T = 1.2Ω, the total effective series damping resistance is $R_t = R_M + R_T$ = 2.45Ω, so from Eq. (37) Q_t = 4.61. Then, from Eq. (35), the effective peaking factor is Q' = 1.37 → 3db. Next, from Eq.

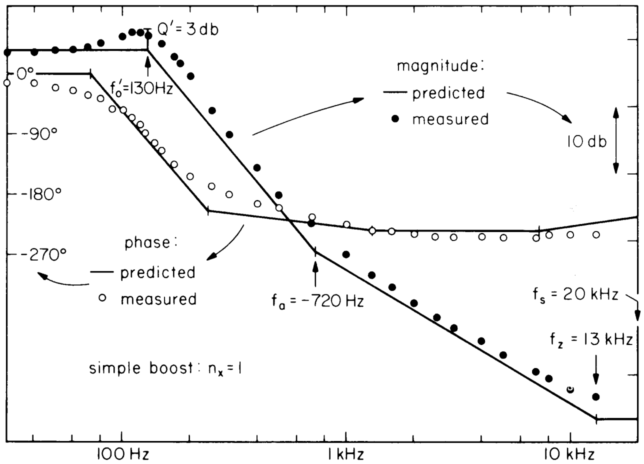

Fig. 20. Exposure of effect of right half-plane zero ω_a on the control describing function in the circuit of Fig. 17 with $n_x = 1$ and D = 0.6: the maximum phase lag exceeds 180°.

(33), $f_z = Q_c f_o = 41 \times 310 = 13$kHz, and from Eq. (34) (with $n_x = 1$ and $D_x = 1$) $f_a = -D'^2 Q_L f_o = -0.4^2 \times 14 \times 310 = -720$Hz. Thus, all the parameters in the control frequency response of Eq. (31) are known, and the corresponding predicted magnitude and phase asymptotes are shown in Fig. 20 for comparison with the measured data points. It is seen that agreement is quite good; in particular, it may be noted that the phase exceeds 180° lag as is expected from the right half-plane zero f_a; the phase fails to reach 270° lag because of the left half-plane zero ω_z due to the capacitance esr.

Further series of measurements were made on the circuit of Fig. 17 in the tapped-inductor condition with $n_x = 2$. A first set of data points for the control describing function $\hat{v}/\hat{v}_2$ was taken under the conditions $f_s = 20$kHz, D = 0.25, V = 25v, and R = 240Ω, and the results are shown in curve (a) in Fig. 21. As in the previous example with $n_x = 1$, the $\hat{v}/\hat{v}_2$ characteristic does not include the effect of R_M, so that a direct measurement of the parasitic loss resistance may be obtained. From curve (a) in Fig. 21, the measured effective peaking factor is Q' = 9db → 2.82, and $Q_c = 41$ and $Q_L = 21$ as in the example with $n_x = 1$. Therefore, from Eq. (35), $Q_t = 4.9$ and hence $R_T = 2.3\Omega$. Since the normalizing frequency is $f_o = 310$Hz, the effective filter corner frequency is $f_o' = D'f_o = 230$Hz.

The actual control describing function $\hat{v}/\hat{v}_1$ was then measured under the same conditions, so that the effect of R_M was included, and the results are shown in curve (b) in Fig. 21. The predicted value of R_M is obtained from Eq. (26), $R_M = n_x^2 V/D_x I_M$: for $f_s = 20$kHz, $I_M = 20$ amps as before; for $n_x = 2$ and D = 0.25, $D_x = Dn_x + D' = (0.25 \times 2) + 0.75 = 1.25$, so for V = 25v, $R_M = (2^2 \times 25)/(1.25 \times 20) = 4.0\Omega$. The predicted value of the total effective series damping

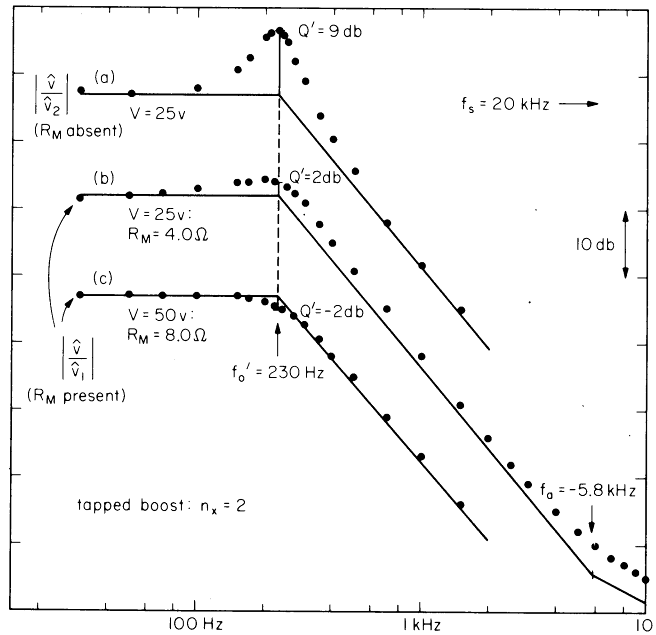

Fig. 21. Exposure of effect of R_M and the right half-plane zero ω_a on the control describing function in the circuit of Fig. 17 with $n_x = 2$ and D = 0.25: (a) determination of $R_T = 2.3\Omega$ from observed Q' = 9db; (b), (c) predicted lower Q' when various calculated values of R_M are included, and observed data points.

resistance is then $R_t = R_M + R_T = 4.0 + 2.3 = 6.3\Omega$, which leads to $Q_t = 1.81$ and a total effective peaking factor Q' = 1.22 → 2db, in good agreement with the observed value in curve (b) of Fig. 21. From Eq. (34), the right half-plane zero is $f_a = -(n_x D'^2 Q_L / D_x) f_o = -(2 \times 0.75^2 \times 21/1.25)310 = -5.8$kHz, also in good agreement with curve (b) of Fig. 21.

As a further check on the model, the previous set of measurements was repeated with all dc levels doubled, so that V = 50v. The results are shown in curve (c) in Fig. 21; the only predicted change is that R_M is doubled because V is doubled, so $R_M = 8.0\Omega$. Then, $R_t = 8.0 + 2.3 = 10.3\Omega$ so $Q_t = 1.1$ which leads to Q' = 0.77 → -2db, in good agreement with curve (c) of Fig. 21.

Finally, some sets of measurements of the control describing function were made for the generalized tapped-inductor boost converter with an input filter. The experimental circuit with inductor tap at $n_x = 2$ is shown in Fig. 22, and the transistor drive conditions and the converter inductor and capacitor were the same as in Fig. 17. Independent measurements led to the input filter element values $L_s = 3.2$mh, $C_s = 12\mu$f, $R_s = 3.5\Omega$ including the capacitor esr. The switching frequency was 20kHz.

Prediction of results from the circuit of Fig. 22 can be made from the general con-

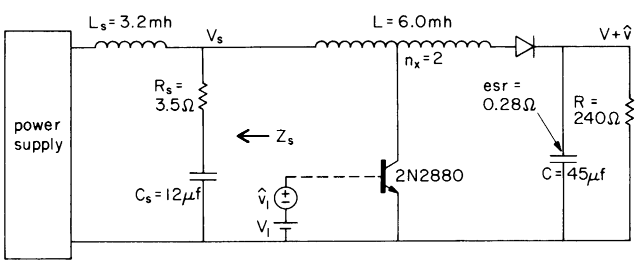

Fig. 22. Experimental tapped-inductor boost converter with input filter.

tinuous model of Fig. 13. The dc and line transmission characteristics are straightforward and will not be discussed further. The nature of the control describing function is not quite so obvious, and understanding of its salient qualitative form is facilitated by some further steps in reduction of the model in order to find a simple equivalent driving generator proportional to the ac duty ratio $\hat{d}$.

Figures 23 and 24 show reduced forms of the general ac model of Fig. 13 that are analogous to those of Figs. 14 and 15, but with retention of the input filter whose effect is represented by its source impedance Z_s looking back into

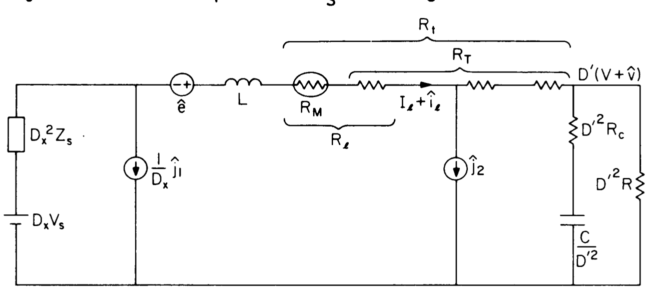

Fig. 23. Partially reduced version of averaged model of Fig. 13 for determination of the control describing function $\hat{v}/\hat{d}$, with input filter.

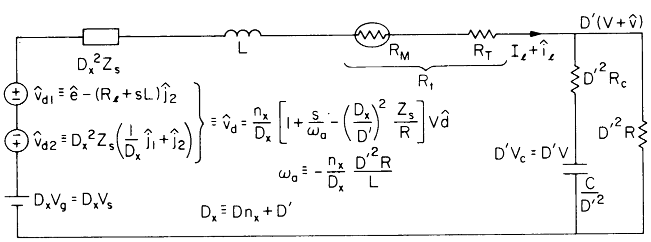

Fig. 24. Fully reduced version of model of Fig. 23, showing appearance of a minimum or possibly a null in the effective driving signal $\hat{v}_d$, in the neighborhood of the input filter resonant frequency ω_s where Z_s reaches a maximum.

the power supply as indicated in Fig. 22. As seen from Fig. 24, the total effective driving generator $\hat{v}_d$ consists of the generator $\hat{v}_{d1}$, previously identified in Fig. 15 as

$$\hat{v}_{d1} = \hat{e} - (R_\ell + sL)\hat{j}_2 \tag{43}$$

$$= \frac{n_x}{D_x}\left(1 + \frac{s}{\omega_a}\right)V\hat{d} \tag{44}$$

and an additional generator $\hat{v}_{d2}$ resulting from the presence of Z_s given by

$$\hat{v}_{d2} = D_x^2 Z_s\left(\frac{1}{D_x}\hat{j}_1 + \hat{j}_2\right) \tag{45}$$

From Eqs. (4) and (5), this generator can be expressed as

$$\hat{v}_{d2} = D_x^2 Z_s \frac{n_x}{D_x}\frac{V}{D'^2 R}\hat{d} \tag{46}$$

in which the dc relation $I_\ell = V/D'R$ has been used. Hence, the total effective driving generator in Fig. 24 is

$$\hat{v}_d = \frac{n_x}{D_x}\left[1 + \frac{s}{\omega_a} - \left(\frac{D_x}{D'}\right)^2 \frac{Z_s}{R}\right]V\hat{d} \tag{47}$$

With substitution for the frequency dependence of the source impedance Z_s, Eq. (47) becomes

$$\frac{\hat{v}_d}{V\hat{d}} = \frac{n_x}{D_x}\left[1 + \frac{s}{\omega_a} - \left(\frac{D_x}{D'}\right)^2 \frac{R_s}{R}\,\frac{Q_s\left(\frac{s}{\omega_s}\right)\left[1 + \frac{1}{Q_s}\left(\frac{s}{\omega_s}\right)\right]}{1 + \frac{1}{Q_s}\left(\frac{s}{\omega_s}\right) + \left(\frac{s}{\omega_s}\right)^2}\right] \tag{48}$$

where

$$\omega_s \equiv \frac{1}{\sqrt{L_s C_s}} \quad (49) \qquad Q_s \equiv \frac{\omega_s L_s}{R_s} \quad (50)$$

The salient features of the control describing function in the presence of the input filter can now be seen by inspection of the reduced model of Fig. 24, and Eq. (48). The source impedance Z_s goes through a maximum value of about Q_s^2/R_s at approximately its resonant frequency ω_s, so that $\hat{v}_d$ goes through a corresponding minimum value. In fact, the minimum could actually be a null if conditions are such that

$$1 - \left(\frac{D_x}{D'}\right)^2 \frac{R_s}{R} Q_s^2 \approx 0 \tag{51}$$

This condition is a function of dc duty ratio D. For the numerical values in the experimental circuit of Fig. 22, $Q_s = 4.66$ and Eq. (51) predicts that a null should occur at $D \approx 0.28$. Computer solution of the model of Fig. 24 with $\hat{v}_d$ given by Eq. (48) showed that a null in the control describing function $\hat{v}/\hat{d}$ actually occurred at $D = 0.29$. Further insight into the results was obtained by computer solution for the pole-zero locations of the control describing function for this value of D and for another on either side of this value, namely D = 0.20, 0.29, and 0.5. Numerical values used were V_s = 14v for D = 0.20, 0.29 and V_s = 9.9v for D = 0.5; $R_M = V/I_M$ with

I_M = 20 amps; and the value R_T = 2.3Ω previously determined for the n_x = 2 converter was used for all three values of D, even though its value actually varies slightly with D.

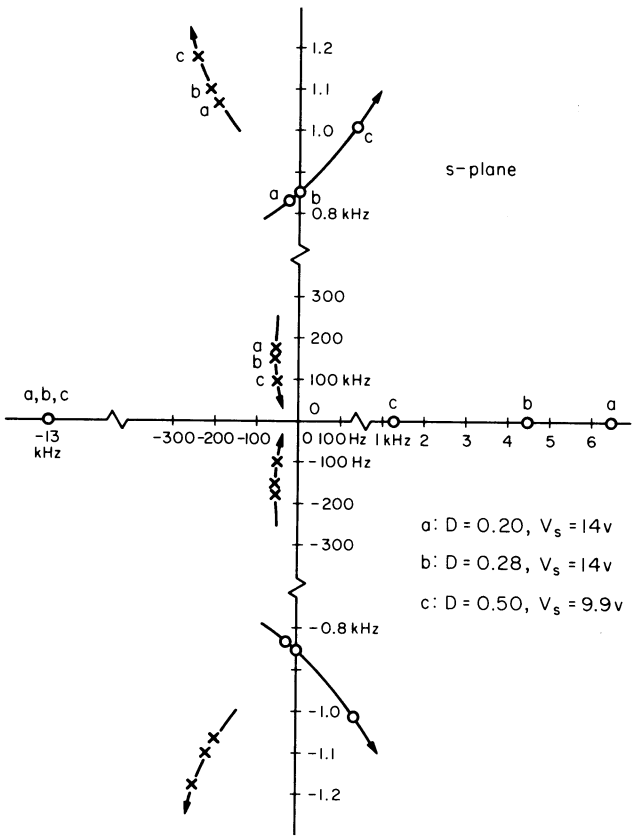

Fig. 25. Computer-calculated pole-zero pattern in the s-plane for the control describing function $\hat{v}/\hat{d}$ obtained from the model of Fig. 24 for the circuit of Fig. 22. A null occurs at D = 0.29 when the complex zero pair crosses the imaginary axis.

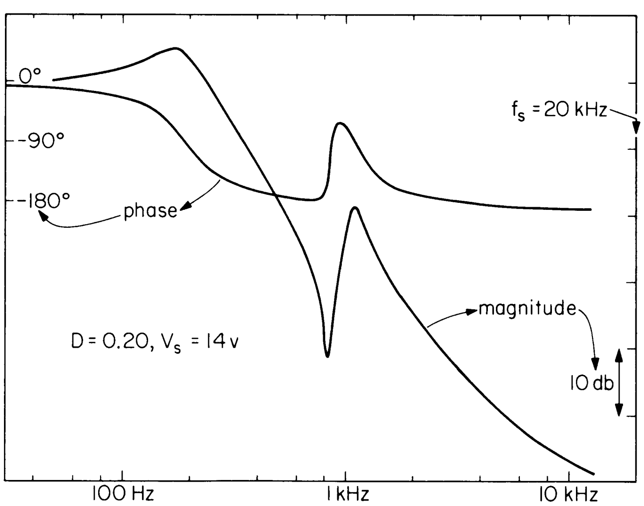

Fig. 26. Computer-calculated magnitude and phase of the control describing function for pole-zero pattern (a) in Fig. 25, showing the minimum in the magnitude response.

The results for the pole-zero positions are shown in Fig. 25. The left half-plane zero, lower-frequency complex pole pair, and the right half-plane zero represent the basic response of the converter effective low-pass filter, with the expected position-dependence upon D. The higher-frequency complex pole pair and complex zero pair represent the response due to the input filter, whose positions also depend upon D. In particular, it is noted that the complex

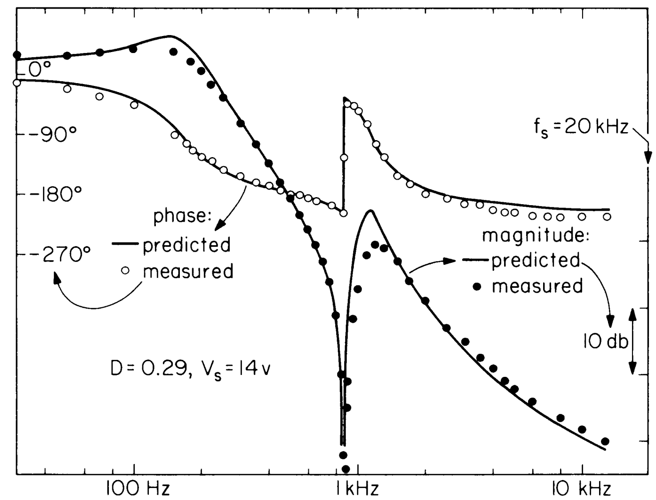

Fig. 27. Computer-calculated magnitude and phase of the control describing function for pole-zero pattern (b) in Fig. 25, and data points obtained from the experimental circuit of Fig. 22, showing the null in the magnitude response.

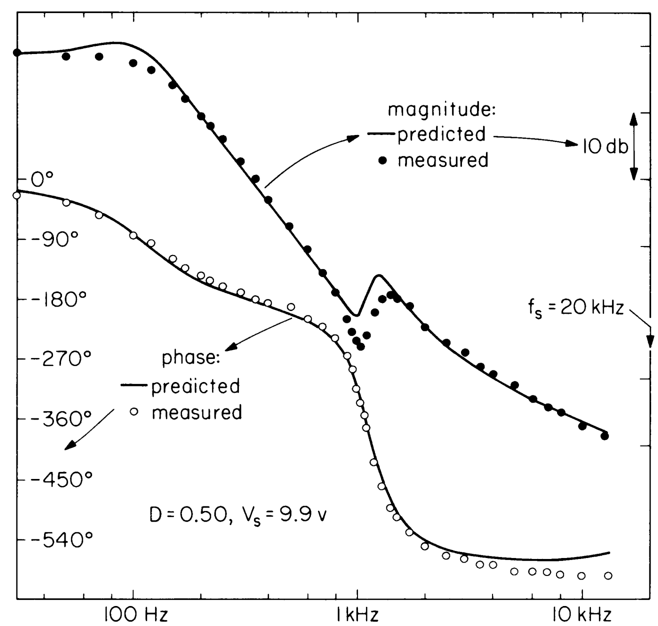

Fig. 28. Computer-calculated magnitude and phase of the control describing function for pole-zero pattern (c) in Fig. 25, and data points obtained from the experimental circuit of Fig. 22, showing the large phase lag at high frequencies.

zero pair crosses from the left half-plane to the right half-plane as D increases, with the expected null at D = 0.29.

The magnitude and phase plots corresponding to the three sets of computed pole-zero positions are shown in Figs. 26 through 28. Data points directly measured in the circuit of Fig. 22 are also shown for two of the sets of conditions.

It is seen that good agreement is obtained between the measured results and the prediction of the model of Fig. 24. From a practical point of view, the chief significance is that a minimum in the control describing function can exist as a consequence of the presence of an input filter, and for a certain dc duty ratio the minimum could become a null. It is noteworthy that a null can occur in spite of finite Q_s (nonzero R_s) in the input filter. Thus, if such a converter were part of a regulator, normal internal adjustment of the dc duty ratio could cause a null in the loop gain. Even more serious, values of dc duty ratio D greater than that for which the null occurs lead to a very large phase lag at high frequencies, much larger than for smaller values of D. This is a consequence of the movement of the complex zero pair from the left half-plane to the right half-plane. Therefore, very severe regulator stability problems could be experienced unless great care is exercised in the design.

5. CONCLUSIONS

A small-signal, low-frequency, averaged model for the tapped-inductor boost converter with input filter has been developed and experimentally verified. The general model is shown in Fig. 13, and from it the dc transfer function and the ac line and control describing functions can be obtained.

The model of Fig. 13 is obtained principally by manipulations of the circuit diagrams rather than by algebraic analysis, so that physical insight into the significance of the steps is retained throughout the derivation. In the absence of an input filter, the ac line and control describing functions are characterized by an effective low-pass filter described by a pair of left half-plane poles and a left half-plane zero; the control describing function has in addition a right half-plane zero. The positions of the poles and of the right half-plane zero change with dc duty ratio D.

The method of derivation of the averaged model is a refinement of that described for the simple boost converter in [1]; the refinement leads to a more accurate representation of the parasitic loss resistances in the model, and was an attempt to explain experimentally measured values of the effective filter Q-factor that were substantially lower than those predicted by the original model. However, it was found that this refinement provided insufficient quantitative correction, and that instead an entirely different effect was responsible for these lower Q-factors.

This new effect is shown to be due to storage-time modulation in the transistor power switch, in which the effective duty ratio modulation at the collector is different from the driving duty ratio modulation at the base. The model of Fig. 13 incorporates this effect in a modulation resistance R_M, which is shown enclosed in an oval as a reminder that it is to be included in the ac model only. The significance of this result is that the modulation resistance R_M contributes to the effective filter ac damping resistance but does not contribute to the effective dc loss resistance; consequently, the filter Q-factor is lowered, but the converter efficiency is unaffected, by the presence of the modulation resistance R_M. This result may be considered a rare exception to Murphy's law, since the storage-time modulation effect produces a desirable damping effect without an associated undesirable loss of efficiency.

Experimental measurements of both magnitude and phase of the control describing function are presented to verify the averaged model both qualitatively and quantitatively. Experimental conditions were chosen specifically to expose certain features of the model for individual verification: for the simple boost converter of Fig. 17 with n_x = 1, Fig. 19 shows the damping effect due to the modulation resistance R_M and Fig. 20 exposes the right half-plane zero and associated excess phase lag; Fig. 21 shows the effect of R_M in the tapped-inductor converter with n_x = 2.

Experimental results are also presented for the control describing function of the system of Fig. 22, a tapped-inductor boost converter with n_x = 2 and with an input filter. The corresponding averaged model is shown in Fig. 24, and the important feature is that the control describing function acquires a complex pair of zeros that can move from the left half-plane to the right half-plane as the dc duty ratio D is increased, as would happen during normal adjustment in a practical closed-loop regulator. The significance of this is illustrated in the magnitude and phase results of Figs. 26 through 28, in which the magnitude plot has a minimum, in the neighborhood of the input filter resonant frequency, which actually becomes a null when the complex pair of zeros lies on the imaginary axis. Furthermore, as the pair of zeros moves into the right half-plane, the magnitude null retreats to a minimum but the phase lag becomes exceedingly large. Unless recognized and properly accounted for, this effect could have disastrous effects upon the stability of a closed-loop regulator.

The physical insight into the nature of the properties of a tapped-inductor boost converter makes the averaged model a useful and easily applied design tool. The method of model derivation can be applied in a similar manner to numerous other circuit configurations.

Thanks are due to Howard Ho and Alan Cassel, graduate students of the California Institute of Technology, for their assistance in constructing the experimental converters and for the computer plots shown in Figs. 26 through 28.

REFERENCES

[1] G. W. Wester and R. D. Middlebrook, "Low-Frequency Characterization of Switched dc-dc Converters," IEEE Power Processing and Electronics Specialists Conference, 1972 Record pp. 9-20; also, IEEE Trans. Aerospace and Electronic Systems, vol. AES-9, no. 3, pp. 376-385, May 1973.

[2] C. L. Searle et al, Elementary Circuit Properties of Transistors, SEEC vol. 3, p. 284; John Wiley & Sons, 1964.

[3] R. D. Middlebrook, "Measurement of Loop Gain in Feedback Systems," International Journal of Electronics, vol. 38, no. 4, pp. 485-512, April 1975.