

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

DESCRIPTION

The PLS100 (3-State) and PLS101 (Open Collector) are bipolar, fuse Programmable Logic Arrays (PLAs). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs and be ANDed together to comprise one P-term. All 48 P-terms can be selectively ORed to each output.

The PLS100 and PLS101 are fully TTL compatible, and chip enable control for expansion of input variables and output inhibit. They feature either Open Collector or 3-State outputs for ease of expansion of product terms and application in bus-organized systems.

Order codes are listed in the Ordering Information Table.

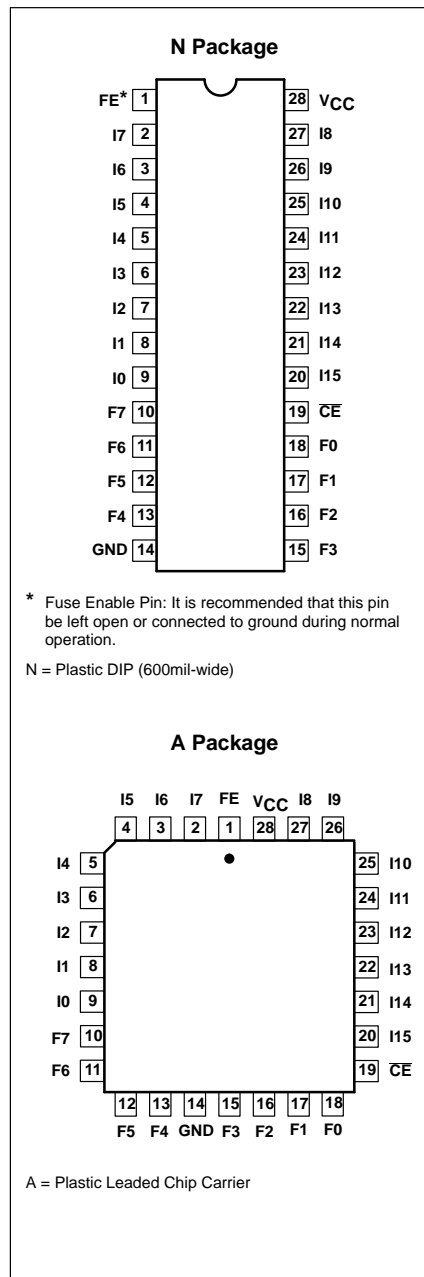
FEATURES

- Field-programmable (Ni-Cr link)
- Input variables: 16
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 50ns (max.)
- Power dissipation: 600mW (typ.)
- Input loading: -100µA (max.)
- Chip Enable input
- Output option:
 - PLS100: 3-State
 - PLS101: Open-Collector
- Output disable function:
 - 3-State: Hi-Z
 - Open-Collector: High

APPLICATIONS

- CRT display systems
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Data security encoders
- Fault detectors
- Frequency synthesizers
- 16-bit to 8-bit bus interface
- Random logic replacement

PIN CONFIGURATIONS



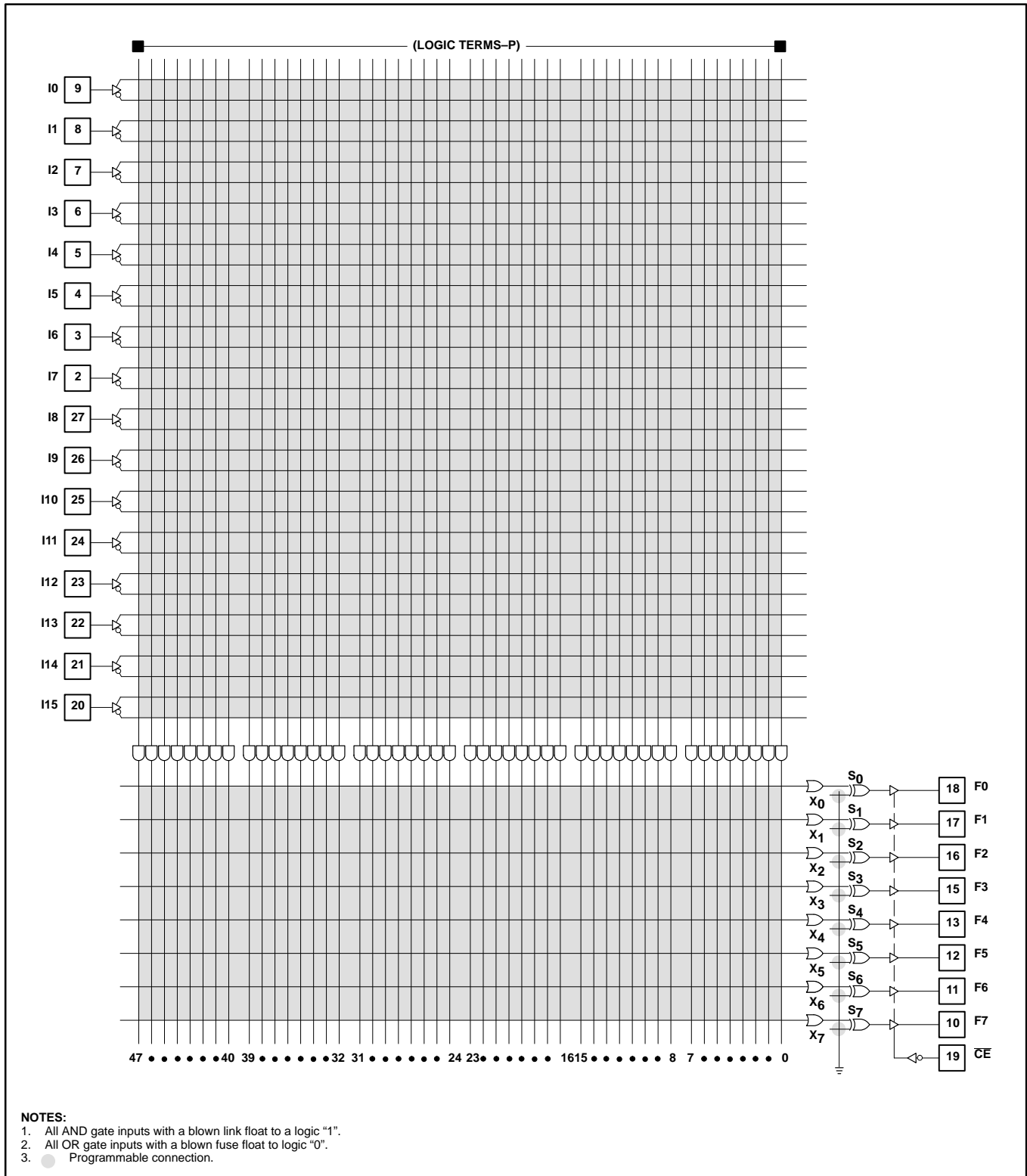
ORDERING INFORMATION

DESCRIPTION	3-STATE	OPEN COLLECTOR	DRAWING NUMBER
28-Pin Plastic Dual In-Line 600mil-wide	PLS100N	PLS101N	0413D
28-Pin Plastic Leaded Chip Carrier	PLS100A	PLS101A	0401F

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

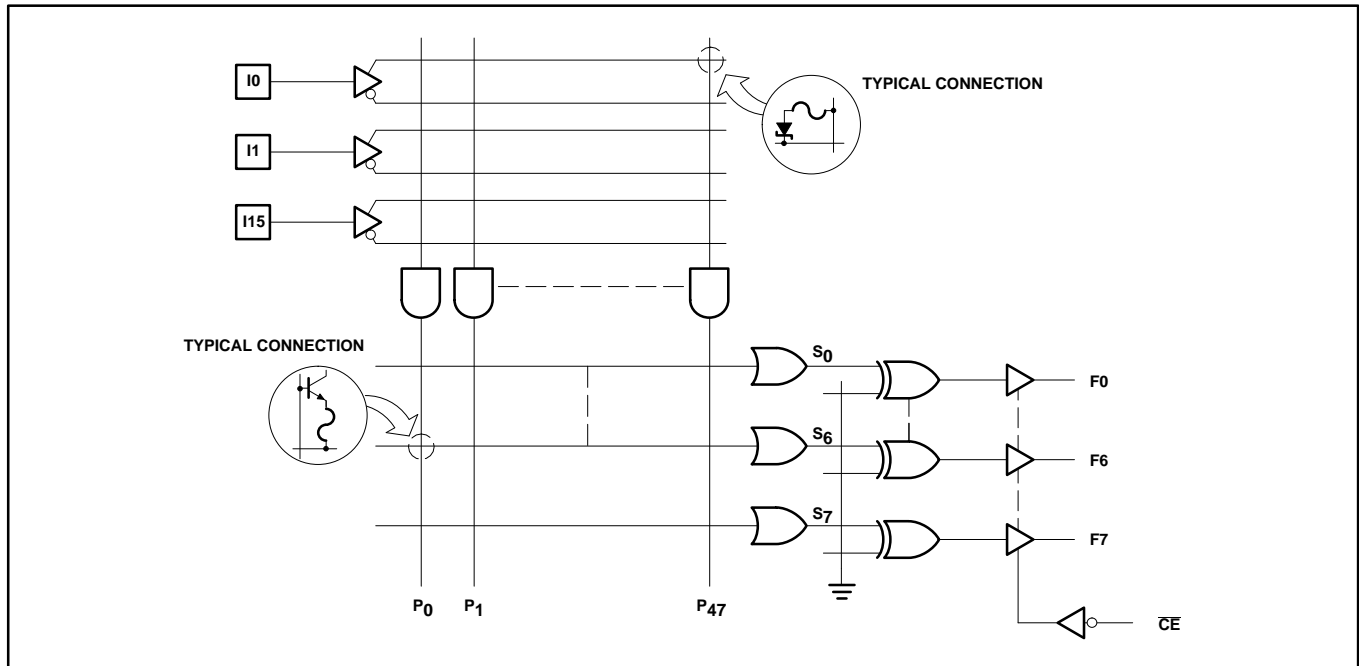
LOGIC DIAGRAM



Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATINGS	UNIT
V _{CC}	Supply voltage	+7.0	V _{DC}
V _{IN}	Input voltage	+5.5	V _{DC}
V _O	Output voltage	+5.5	V _{DC}
I _{IN}	Input current	±30	mA
I _{OUT}	Output current	+100	mA
T _{amb}	Operating temperature range	0 to +75	°C
T _{stg}	Storage temperature range	-65 to +150	°C

NOTE:

- Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS100 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Philips Semiconductors Military Data Handbook.

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

DC ELECTRICAL CHARACTERISTICS

 $0^{\circ}\text{C} \leq T_{\text{amb}} \leq +75^{\circ}\text{C}$, $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ¹	MAX	
Input voltage²						
V_{IH}	High	$V_{\text{CC}} = \text{MAX}$	2.0			V
V_{IL}	Low	$V_{\text{CC}} = \text{MIN}$			0.8	V
V_{IC}	Clamp ³	$V_{\text{CC}} = \text{MIN}$, $I_{\text{IN}} = -12\text{mA}$		-0.8	-1.2	V
Output voltage²						
V_{OH}	High (PLS100) ⁴	$V_{\text{CC}} = \text{MIN}$ $I_{\text{OH}} = -2\text{mA}$	2.4			V
V_{OL}	Low ⁵	$I_{\text{OL}} = 9.6\text{mA}$		0.35	0.45	V
Input current						
I_{IH}	High	$V_{\text{IN}} = 5.5\text{V}$		< 1	25	μA
I_{IL}	Low	$V_{\text{IN}} = 0.45\text{V}$		-10	-100	μA
Output current						
$I_{\text{O(OFF)}}$	Hi-Z state (PLS100)	$\overline{\text{CE}} = \text{High}$, $V_{\text{CC}} = \text{MAX}$ $V_{\text{OUT}} = 5.5\text{V}$		1	40	μA
I_{OS}	Short circuit (PLS100) ^{3, 6}	$V_{\text{OUT}} = 0.45\text{V}$ $\overline{\text{CE}} = \text{Low}$, $V_{\text{OUT}} = 0\text{V}$	-15	-1	-40	μA
I_{CC}	V_{CC} supply current ⁷	$V_{\text{CC}} = \text{MAX}$		120	170	mA
Capacitance						
C_{IN}	Input	$\overline{\text{CE}} = \text{High}$, $V_{\text{CC}} = 5.0\text{V}$ $V_{\text{IN}} = 2.0\text{V}$		8		pF
C_{OUT}	Output	$V_{\text{OUT}} = 2.0\text{V}$		17		pF

NOTES:

- All typical values are at $V_{\text{CC}} = 5\text{V}$, $T_{\text{amb}} = +25^{\circ}\text{C}$.
- All voltage values are with respect to network ground terminal.
- Test one pin at a time.
- Measured with V_{IL} applied to $\overline{\text{CE}}$ and a logic high stored.
- Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC} .
- Duration of short circuit should not exceed 1 second.
- I_{CC} is measured with the Chip Enable input grounded, all other inputs at 4.5V and the outputs open.

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

AC ELECTRICAL CHARACTERISTICS

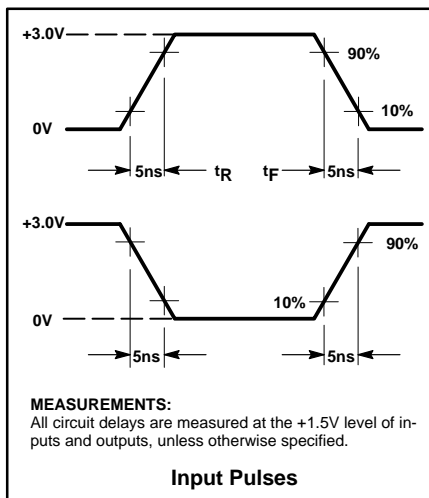
0°C ≤ T_{amb} ≤ +75°C, 4.75 ≤ V_{CC} ≤ 5.25V, R₁ = 470Ω, R₂ = 1kΩ

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				MIN	TYP ¹	MAX	
Propagation delay²							
t _{PD}	Input	Output	Input		35	50	ns
t _{CE}	Chip Enable ³	Output	Chip Enable		15	30	ns
Disable time							
t _{CD}	Chip Disable ³	Output	Chip Enable		15	30	ns

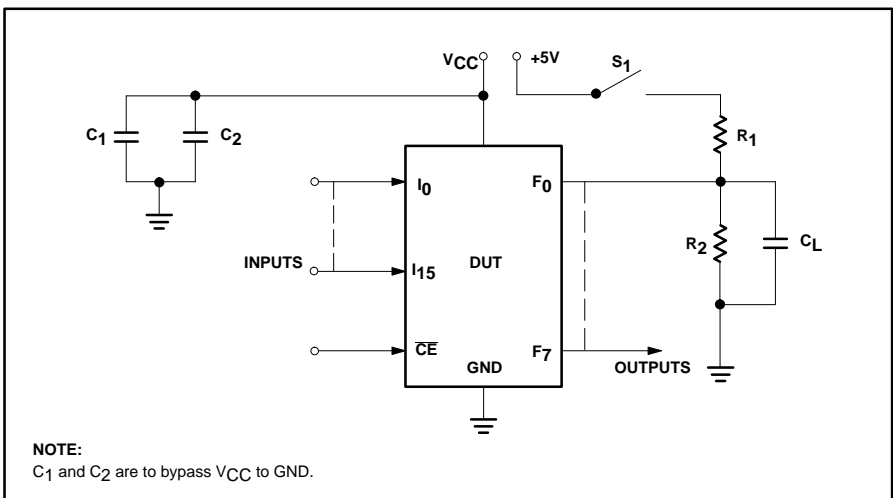
NOTES:

1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All propagation delays are measured and specified under worst case conditions.
3. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S₁ is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of V_T = (V_{OH} - 0.5V) with S₁ open, and Low-to-High impedance tests are made to the V_T = (V_{OL} + 0.5V) level with S₁ closed.

VOLTAGE WAVEFORMS



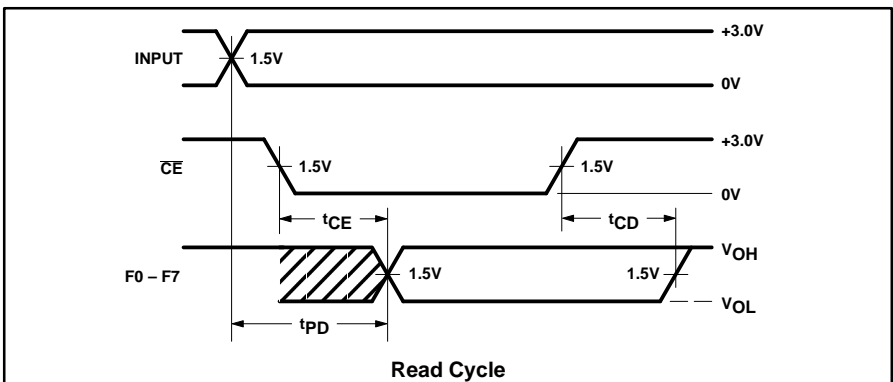
TEST LOAD CIRCUIT



TIMING DEFINITIONS

SYMBOL	PARAMETER
t _{CE}	Delay between beginning of Chip Enable Low (with Input valid) and when Data Output becomes valid.
t _{CD}	Delay between when Chip Enable becomes High and Data Output is in off state (Hi-Z or High).
t _{PD}	Delay between beginning of valid Input (with Chip Enable Low) and when Data Output becomes valid.

TIMING DIAGRAM



Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

LOGIC PROGRAMMING

PLS100/PLS101 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors' SNAP, Data I/O Corporation's ABEL™ and Logical Devices Inc.'s CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

PLS100/PLS101 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Philips Semiconductors' SNAP PLD design software package.

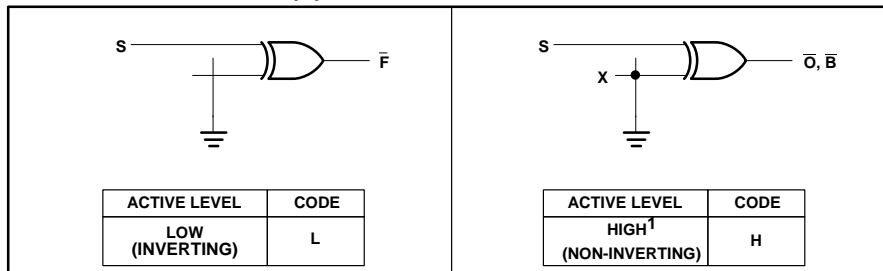
To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE,

COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

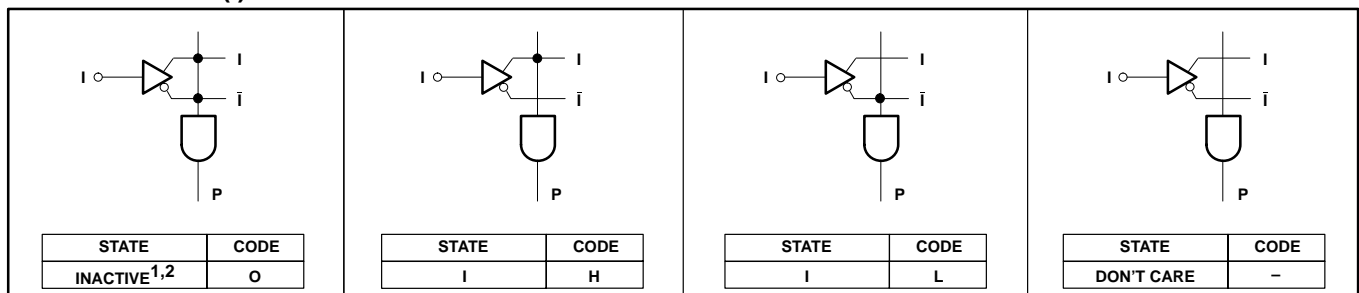
PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 (*Development Software*) and Section 10 (*Third-party Programmer/Software Support*) of this data handbook for additional informational.

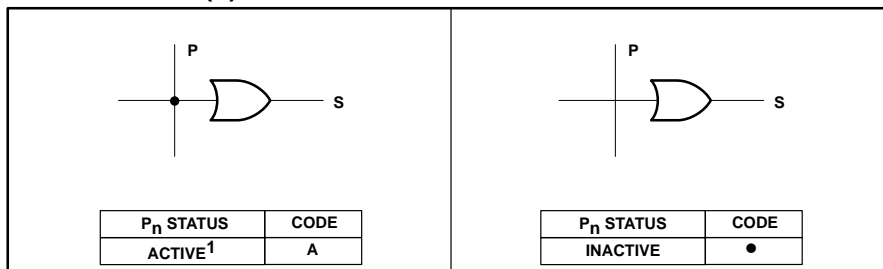
OUTPUT POLARITY – (F)



“AND” ARRAY – (I)



“OR” ARRAY – (F)



NOTES:

1. This is the initial unprogrammed state of all links. It is normally associated with all unused (inactive) AND gates P_n.
2. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

VIRGIN STATE

The PLS100/101 virgin devices are factory shipped in an unprogrammed state, with all fuses intact, such that:

1. All P_n terms are disabled (inactive) in the AND array.
2. All P_n terms are active in the OR array.
3. All outputs are Active-High.

ABEL is a trademark of Data I/O Corp.
CUPL is a trademark of Logical Devices, Inc.

Programmable logic arrays (16 × 48 × 8)

PLS100/PLS101

SNAP RESOURCE SUMMARY DESIGNATIONS

